ESPRESSIF

Compatibility Advisory

Title	Compatibility Advisory for ESP32-C3 Chip Revision v1.1
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Serial Number	NA
Version	V1.1

Introduction

To gain more usable SRAM space for project application development with ESP32-C3 chip, we have upgraded the ESP32-C3 chip to revision v1.1. This latest chip revision, when paired with an upgraded ESP-IDF version, provides approximately 10 KB[1] of additional SRAM space.

The increase in available SRAM space is made available by updating ROM code to place more runtime-required code in ROM, instead of a physical SRAM size change.

Given that the addresses and other aspects of the ROM functions for chip revision v1.1 have changed significantly, the binary compiled (hereinafter referred to as firmware) with earlier versions of ESP-IDF cannot run directly on chip revision v1.1. It is necessary to upgrade ESP-IDF to the required version or higher and recompile the firmware.

If you use both chip revision v1.1 and v0.4, it is possible to recompile a binary compatible with both revisions through configurations. However, with such a binary you cannot utilize the 10 KB SRAM space saved through the ROM code updates.

[1]: If the SPI_FLASH_ROM_IMPL option is enabled, an additional 8 KB of SRAM space will be available, so total available SRAM space will increase by 10 KB + 8 KB. Enabling this option is therefore recommended. The value is derived from testing using esp-idf/examples/bluetooth/nimble/bleprph_wifi_coex, and the actual size may vary depending on the specific applications.

Evaluation and Recommendations for Chip Revision Compatibility

In terms of hardware, ESP32-C3 chip revision v1.1 is compatible with earlier revisions. The evaluation is for software compatibility. If you are using chip revisions earlier than v1.1 and plan to switch to chip revision v1.1, it is necessary to upgrade ESP-IDF versions to the required versions and above, as the ESP-IDF version you are using cannot run on chip revision v1.1. To upgrade ESP-IDF for supporting chip revision v1.1, the following scenarios are provided for quick reference.

Scenario	Upgrade ESP-IDF versions to required versions and above	"Minimum Supported ESP32-C3 Revision"	Additional 10 KB SRAM	Notes
Use the same firmware for chip revision v1.1 and earlier revisions, maintaining software compatibility with both revisions	Yes	Rev v0.4	No	This scenario ensures software compatibility with different chip revisions, but the additional SRAM space is not available. If ESP-IDF is not upgraded, the compiled binary cannot run on chip revision v1.1.
Use separate firmware for chip revision and earlier revisions, aiming to utilize the additional SRAM space with chip revision v1.1	Yes	Rev 1.1	Yes	This scenario saves SRAM space on chip revision v1.1 if ESP-IDF is upgraded and configured correctly. Software based on old ESP-IDF versions should still be maintained.

Required ESP-IDF Configurations for Chip Revision v1.1

To use chip revision v1.1 with 10 KB + 8 KB more SRAM space, the following steps are needed:

1. Upgrade ESP-IDF versions according to the table below:

Release branch	Recommended	Required
release/v4.3 (EOL)	v4.3.7+	v4.3.7
release/v4.4 (EOL)	v4.4.7+	v4.4.7
release/v5.0	v5.0.5+	v5.0.5
release/v5.1	v5.1.3+	v5.1.3
release/v5.2 and above	v5.2+	v5.2

2. Set "Minimum Supported ESP32-C3 Revision" in "menuconfig":
    When running the project configuration utility "menuconfig" of ESP-IDF, set
    "Minimum Supported ESP32-C3 Revision" (> Component config > Hardware
    Settings > Chip revision) as "Rev v1.1". The default value is "Rev v0.3".

3. Set "SPI_FLASH_ROM_IMPL" in "menuconfig": When running the project
    configuration utility "menuconfig" of ESP-IDF, set "SPI_FLASH_ROM_IMPL"
    (> Component config > SPI Flash driver > Use esp_flash implementation in
    ROM) to "true". The default value is "false".

```
(Top) → Component config → SPI Flash driver
                    Espressif IoT Development Framework Configuration
[ ] Verify SPI flash writes
[ ] Enable operation counters
[*] Enable SPI flash ROM driver patched functions
[ ] Use esp_flash implementation in ROM
    Writing to dangerous flash regions (Aborts)  --->
[ ] Bypass a block erase and always do sector erase
[*] Enables yield operation during flash erase
(20)    Duration of erasing to yield CPUs (ms)
(1)     CPU release time (tick) for an erase operation
(8192) Flash write chunk size
[ ] Override flash size in bootloader header by ESPTOOLPY_FLASHSIZE
[ ] Flash timeout checkout disabled
[ ] Override default chip driver list
    Auto-detect flash chips  --->
[*] Enable encrypted partition read/write operations




[Space/Enter] Toggle/enter   [ESC] Leave menu        [S] Save
[O] Load                     [?] Symbol info         [/] Jump to symbol
[F] Toggle show-help mode    [C] Toggle show-name mode  [A] Toggle show-all mode
[Q] Quit (prompts for save)  [D] Save minimal config (advanced)
```

4.   Compile and flash the software.

Compatibility with Chip Revision v0.4

The option "Minimum Supported ESP32-C3 Revision" in "menuconfig" specifies the lowest expected compatible chip revision.

If "Minimum Supported ESP32-C3 Revision" in "menuconfig" is set to "Rev v1.1", the software will rely on the newly provided code in the ROM and remove the corresponding 10 KB functions that were originally located in the SRAM. Therefore, the binary file compiled with this option will not be able to run on chip revisions below v1.1.

If two revisions (e.g. chip revision v0.4 and v1.1) need to be used at the same time, the ROM functions should not be removed. "Minimum Supported ESP32-C3 Revision" in "menuconfig" should be set to the lowest revision used (e.g. "Rev 0.4"), and the binary file should be recompiled with this setting. The recompiled binary will be able to run on both chip revisions (e.g. chip revision v0.4 and v1.1), but the additional 10 KB of SRAM space will not be available.

If "Minimum Supported ESP32-C3 Revision" in "menuconfig" is set to "Rev v1.1", and the compiled binary is mistakenly flashed to a chip revision below v1.1, both the download tool (esptool) and the boot code (the second stage bootloader) will report errors. Below is the error message from the esptool tool:

A fatal error occurred: bootloader/bootloader.bin requires chip revision in range [v1.1 - v1.99] (this chip is revision v0.4). Use --force to flash anyway.

Identification of Chip Revisions

For how to identify chip revisions, please refer to ESP32-C3 Series SoC Errata. For explanations of software compatibility, please refer to Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.

Contact

If you need technical assistance, please contact Espressif.

Revision History

Date	Version	Release Notes
2025/04/14	V1.1	1. Clarified the saved SRAM value. 2. Updated "Required ESP-IDF Configurations for Chip Revision v1.1".
2024/07/22	V1.0	Initial release.