ESP32-H2 Series

Hardware Design Guidelines

Introduction

Hardware design guidelines give advice on how to integrate ESP32-H2 into other products. ESP32-H2 is a series of ultra-low-power SoCs with support for Bluetooth® 5 (LE), Bluetooth Mesh, Thread, Matter and Zigbee.

These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif's standards.

Pre-release v0.7
Espressif Systems

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1 Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-h2_hardware_design_guidelines_en.pdf

ESP32-H2 series is a low-power MCU-based SoC solution that supports Bluetooth® 5 (LE), Zigbee 3.0 and Thread 1.3 (802.15.4). With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), smart home, industrial automation, health care, and consumer electronics.

ESP32-H2 has a 32-bit RISC-V processor, operating at up to 96 MHz. The chip supports application development to operate without the need for a host MCU.

ESP32-H2 series provides a highly-integrated way to implement wireless communication technologies using a complete RF subsystem, including a antenna switch, RF balun, power amplifier, low noise amplifier (LNA), filter, power management unit, calibration circuits, etc. As a result, PCB size has been greatly reduced.

With its advanced calibration circuitry, ESP32-H2 series can dynamically adjust itself to remove external circuit imperfections or adapt to changes in external conditions.

For more information about ESP32-H2 series, please refer to *ESP32-H2 Series Datasheet*.

Note:

Unless otherwise specified, "ESP32-H2" used in this document refers to the series of chips, instead of a specific chip variant.

2 Schematic Checklist

The integrated circuitry of ESP32-H2 requires only 17 electrical components (resistors, capacitors, and inductors) and one crystal. The high integration of ESP32-H2 allows for simple peripheral circuit design. This chapter details ESP32-H2 schematics.

ESP32-H2 schematics are shown in Figure 1.

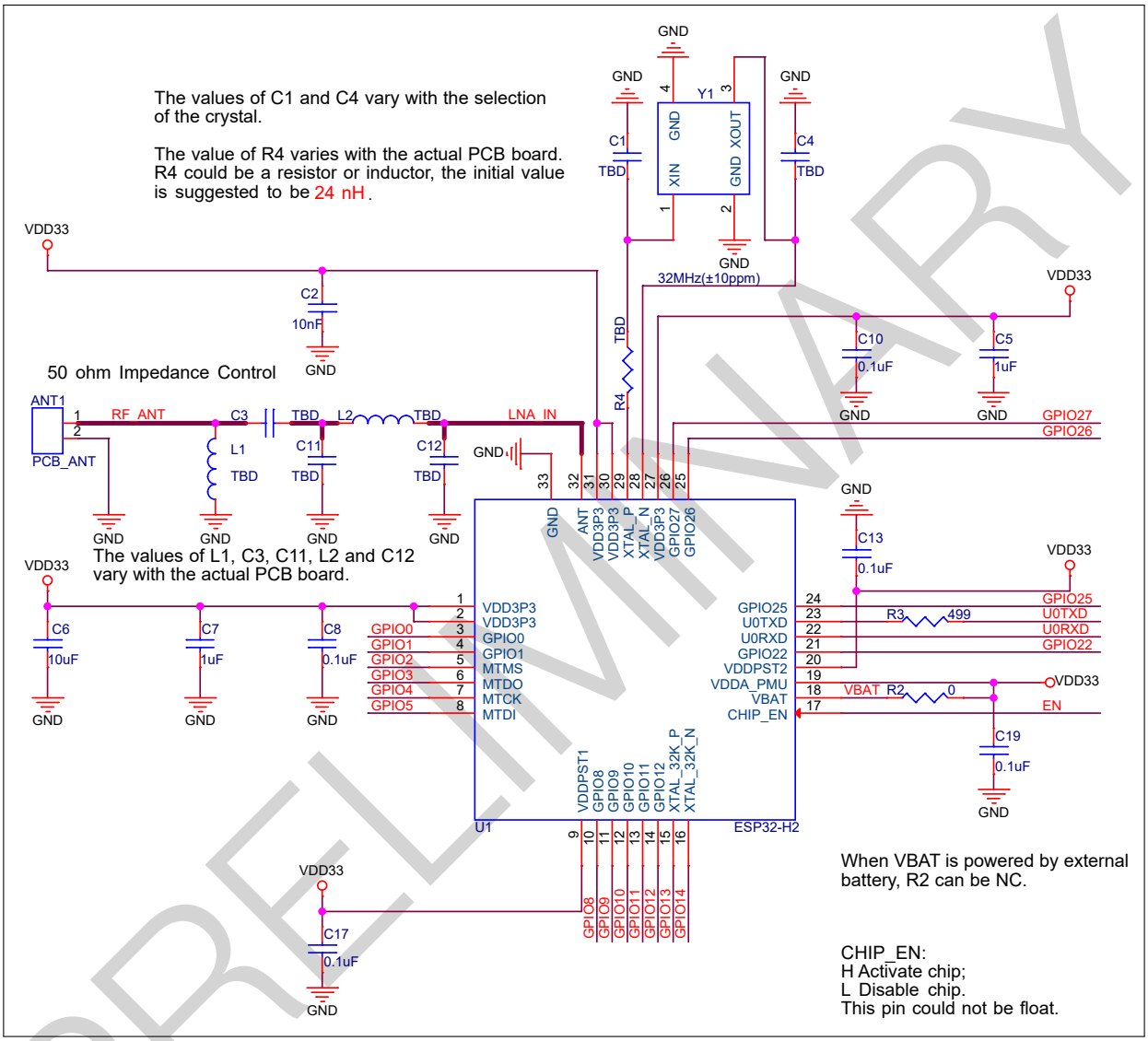

Figure 1: ESP32-H2 Schematic

Any basic ESP32-H2 circuit design may be broken down into 10 major sections:

- Power supply
- Power-on sequence and system reset
- Flash
- Clock source
- RF
- UART
- Strapping pins
- GPIO
- ADC
- USB

The rest of this document details the specifics of circuit design for each of these sections.

2.1 Power Supply

For more information about power pins, please refer to *ESP32-H2 Series Datasheet* > Section Power Supply.

2.1.1 Digital Power Supply

ESP32-H2 has pin9 VDDPST1 and pin20 VDDPST2 that supply power to Group0 IO and Group1 IO respectively, in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 μF filter capacitor close to each digital power supply pin.

The schematic for the digital power supply pins is shown in Figure 2.

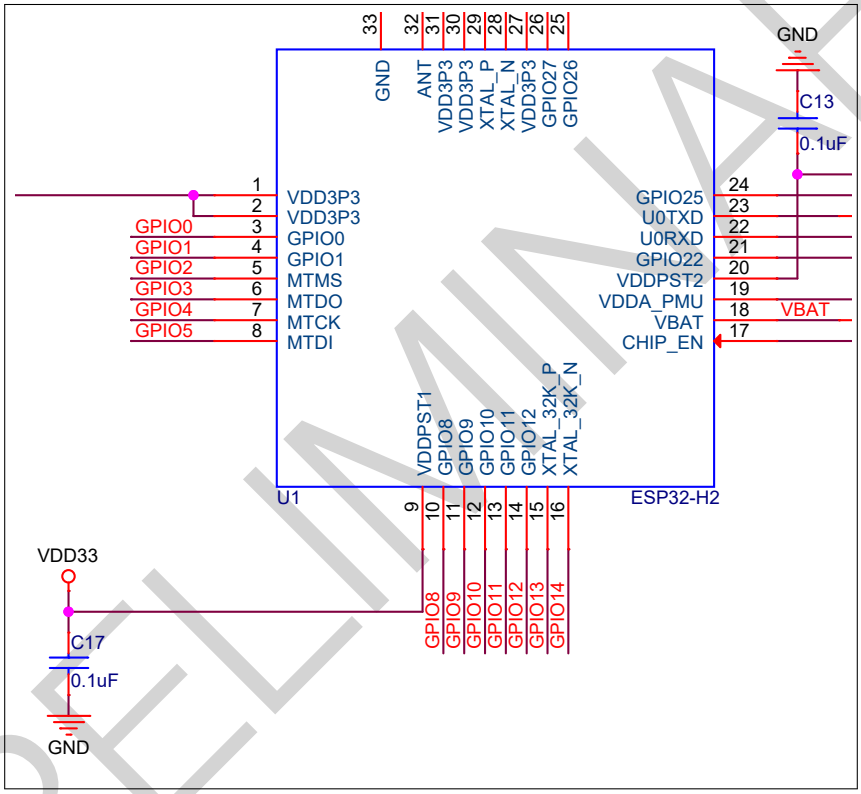

Figure 2: Schematic for the Digital Power Supply Pins

2.1.2 Analog Power Supply

ESP32-H2's pin1 VDD3P3, pin2 VDD3P3, pin18 VBAT, pin19 VDDA_PMU, pin27 VDD3P3, pin30 VDD3P3 and pin31 VDD3P3 are the analog power supply pins, working at 3.0 V ~ 3.6 V.

For pin1 VDD3P3 and pin2 VDD3P3, it should be noted that the sudden increase in current draw, when ESP32-H2 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add another 10 μF capacitor to the power trace, which can work in conjunction with the 1 μF capacitor and the 0.1 μF. Refer to Figure 3 and place the appropriate decoupling capacitor near each analog power pin.

If VBAT is powered separately by an external power supply, R2 is not required and the operating voltage range is 3.0 V to 3.6 V.

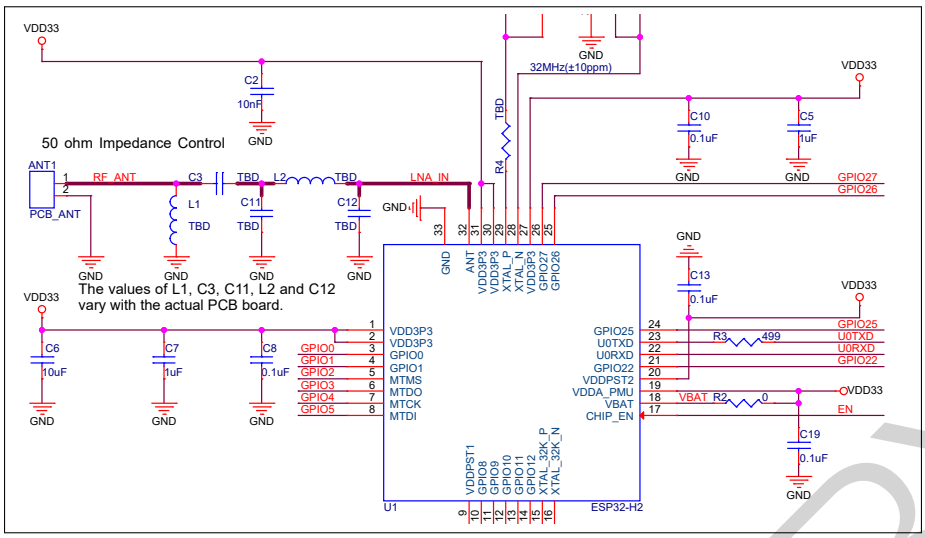

Figure 3: Schematic for the Analog Power Supply Pins

Notice:

- When use the single power supply, the recommended power supply voltage for ESP32-H2 is 3.3 V and the output current is no less than 350 mA.
- It is suggested to add another 10 μF capacitor at the power entrance. If the power entrance is close to pin1 and pin2, it can share the same 10 μF capacitor with pin1 and pin2.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-up Timing and System Reset

2.2.1 Power-up Timing

When ESP32-H2 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_EN is pulled up and the chip is enabled. Therefore, CHIP_EN needs to be powered up after the 3.3 V rails have been brought up. More details about the power-up timing can be found in Section 2.2.3.

Notice:

To ensure the correct power-up timing, it is advised to add an RC delay circuit at the CHIP_EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing sequence of the chip.

2.2.2 System Reset

CHIP_EN serves as the reset pin of ESP32-H2. When CHIP_EN is at low level, the reset voltage (V_{IL_nRST}) should be in the range of (–0.3 ~ 0.25 × VDD) V. To avoid reboots caused by external interferences, make the CHIP_EN trace as short as possible. Also, add a pull-up resistor as well as a capacitor to ground whenever possible. More details can be found in Section 2.2.3.

Notice:

CHIP_EN pin must not be left floating.

2.2.3 Power-up and Reset Timing

Figure 4 shows the power-up and reset timing of ESP32-H2 series of chips. Details about the parameters are listed in Table 1.

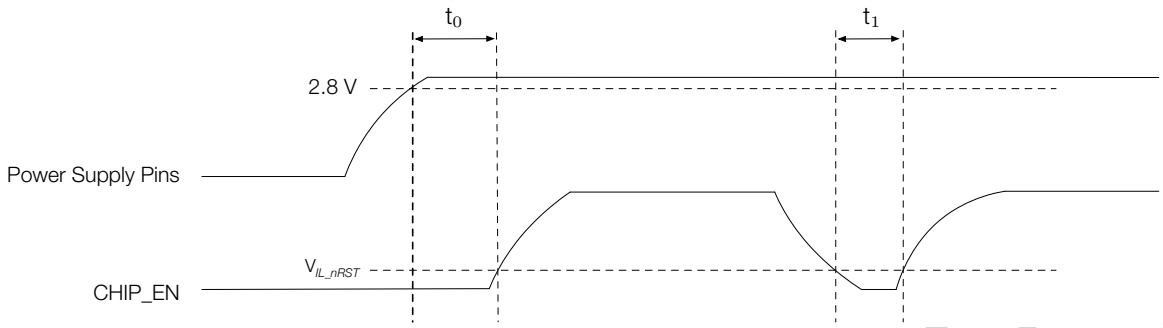

Figure 4: Visualization of Timing Parameters for Power-up and Reset

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_0	Time between bringing up the power supply pins and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} to reset the chip	50

Notice:

If the user application has one of the following scenarios:

- Slow power rise or fall, such as during battery charging or when large capacitors are present in the power supply.
- Frequent power on/off operations.
- Unstable power supply, such as in photovoltaic power generation.

Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:

- Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
- Implementing reset functionality through a button or the main controller.

2.3 Flash

ESP32-H2 series of chips have in-package 2 MB or 4 MB flash. The pins for flash are not bonded out.

2.4 Clock Source

ESP32-H2 has two clock sources:

- External clock source
- RTC clock source

2.4.1 External Clock Source (compulsory)

Currently, the ESP32-H2 firmware only supports 32 MHz crystal.

Crystal

The circuit for the crystal is shown in Figure 5. Note that the accuracy of the selected crystal should be within ±10 ppm.

Please add a series component (resistor or inductor, see R4 in Figure 5) on the XTAL_P clock trace. Initially, it is suggested to use an inductor of **24 nH** to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C4 can be determined according to the formula:

$$C_L = \frac{C1 \times C4}{C1 + C4} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signals with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.
    - When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
    - When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
    - External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

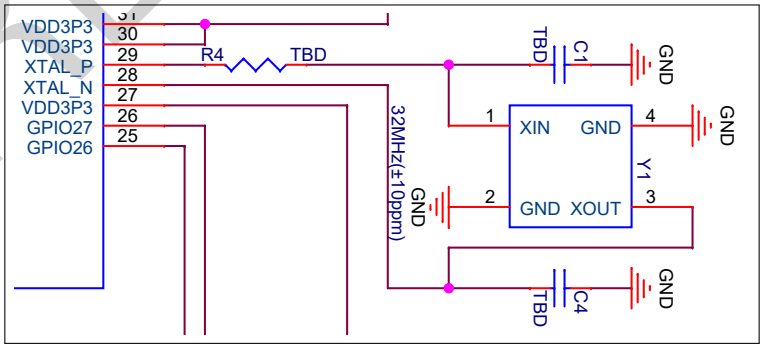

Figure 5: Schematic for the Crystal

Notice:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ±10 ppm, unstable

performance within operating temperature range, etc) may lead to the malfunction of ESP32-H2, resulting in a decrease of the RF performance.

- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

2.4.2 Low-Power Clock(optional)

ESP32-H2 supports an external 32.768 kHz crystal or an external signal (e.g., an oscillator) to act as the low-power sleep clock. Using a low-power clock is aimed at achieving more accurate timekeeping and reducing average power consumption, and does not have impact on the functionality.

Figure 6 shows the schematic for the external 32.768 kHz crystal.

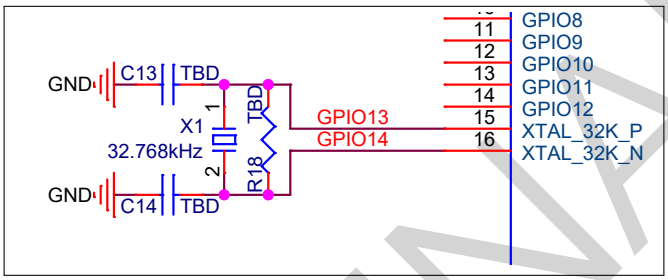

Figure 6: Schematic for the Low-Power Clock

Notice:

- Please note the requirements for the 32.768 kHz crystal.
  - Equivalent series resistance (ESR) $\leqslant 70\ k\Omega$.
  - Load capacitance at both ends should be configured according to the crystal's specification.
- The parallel resistor R is used for biasing the crystal circuit ($5\ M\Omega < R \leqslant 10\ M\Omega$). In general, you do not need to populate the resistor.
- If the Low-Power clock is not required, then the pins for the external 32.768 kHz crystal can be used as other GPIOs.

2.5 RF

The RF circuit of the ESP32-H2 series of chips is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit.

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. It is recommended to use the CLCCL structure to form a bandpass filter, which is mainly used to adjust impedance points, suppress harmonics, and suppress low-frequency noise (especially in applications such as electrical lighting where the effect is significant). If there is no AC-to-DC circuit in the user application, a simpler CLC structure can be considered. The CLCCL matching circuit is shown in Figure 7.
- For the antenna and the antenna matching circuit, to ensure the radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is

recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

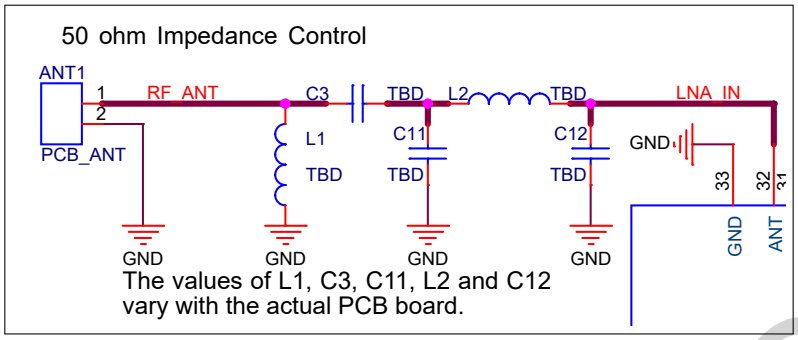

Figure 7: Schematic for RF Matching

Figure 8 shows the general process of RF tuning.

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, and S21 is used to describe the transmission loss of signal from Port 1 to Port 2. For ESP32-H2 series of chips, if S11 is less than or equal to -10 dB and S21 is less than or equal to -35 dB when transmitting 4.8 GHz and 7.2 GHz signals, the matching circuit can satisfy transmission requirements.

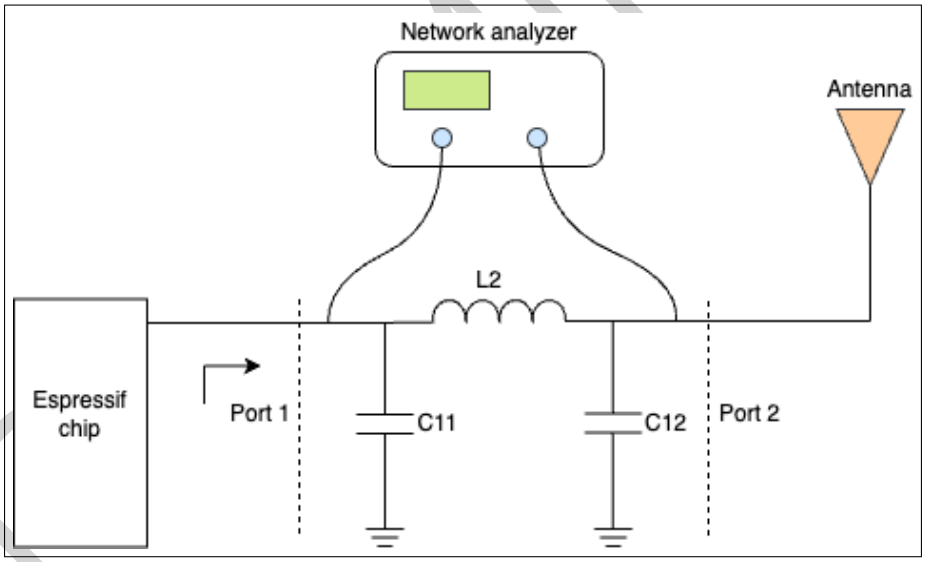

Figure 8: RF Tuning Diagram

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter 3, you can refer to the value ranges in the following to debug the matching circuit:

If the components are in the 0201 SMD package size, please use a stub in the PCB design of the RF matching circuit near the chip. The recommended value ranges for the components are

Reference Designator	Recommended Value	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

If the RF function is not required, the RF pin can be left floating.

If the usage or production environment is sensitive to electrostatic discharge, it is recommended to reserve ESD protection devices near the antenna.

Notice:
The matching parameters vary with the board, so the ones used in our modules could not be applied directly.

2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

Usually UART0 is used as the serial port for download and log printing, and UART0 pins (U0TXD and U0RXD) are fixed. For instructions on download over UART0, please refer to Section 4.3.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

When using the AT firmware, please note that the UART GPIO is already configured (refer to AT Firmware Download). It is recommended to use the default configuration.

2.7 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

All the information about strapping pins is covered in *ESP32-H2 Series Datasheet* > Section *Strapping Pins*.

In this document we will mainly cover the strapping pins related to boot mode.

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 3 Boot Mode Control.

Table 3: Boot Mode Control

Boot Mode	GPIO8	GPIO9
Default Config	– (Floating)	1 (Pull-up)
SPI Boot	Any value	1
Joint Download Boot[1]	1	0

[1] Joint Download Boot mode supports the following download methods:
- USB-Serial-JTAG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

In addition to SPI Boot and Joint Download Boot modes, ESP32-H2 also supports SPI Download Boot mode. For details, please see ESP32-H2 Technical Reference Manual > Chip Boot Control.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 4 and Figure 9.

Table 4: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

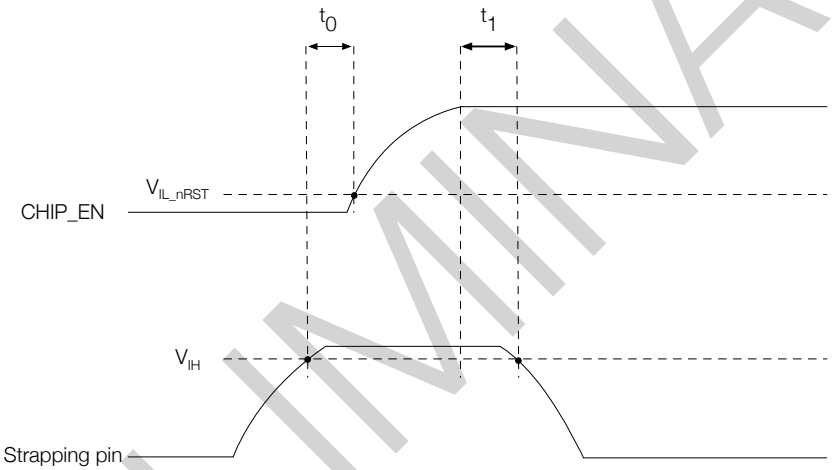

Figure 9: Visualization of Timing Parameters for the Strapping Pins

Notice:
Please do not add high-value capacitors at GPIO9, otherwise the chip not boot successfully.

2.8 GPIO

The pins of ESP32-H2 series can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals can only be routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to *ESP32-H2 Series Datasheet* > Section *Peripheral Pin Configurations*.

When using GPIOs:

- Pay attention to the states of strapping pins during power-up.

- Pay attention to their default configurations after reset (refer to Table 5). It is recommended to add a pull-up or pull-down resistor to pins in high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.

Note:
The content below is excerpted from *ESP32-H2 Series Datasheet* > Section *Pins*.

Table 5: IO MUX Pin Functions

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
GPIO0	3	GPIO0	GPIO0	FSPIQ	0	—
GPIO1	4	GPIO1	GPIO1	FSPICS0	0	R
MTMS	5	MTMS	GPIO2	FSPIWP	1	R
MTDO	6	MTDO	GPIO3	FSPIHD	1	R
MTCK	7	MTCK	GPIO4	FSPICLK	1*	R
MTDI	8	MTDI	GPIO5	FSPID	1	R
GPIO8	10	GPIO8	GPIO8	—	1	—
GPIO9	11	GPIO9	GPIO9	—	3	—
GPIO10	12	GPIO10	GPIO10	—	0	R
GPIO11	13	GPIO11	GPIO11	—	0	R
GPIO12	14	GPIO12	GPIO12	—	0	—
XTAL_32K_P	15	GPIO13	GPIO13	—	0	R
XTAL_32K_N	16	GPIO14	GPIO14	—	0	R
GPIO22	21	GPIO22	GPIO22	—	0	—
U0RXD	22	U0RXD	GPIO23	FSPICS1	3	—
U0TXD	23	U0TXD	GPIO24	FSPICS2	4	—
GPIO25	24	GPIO25	GPIO25	FSPICS3	1	—
GPIO26	25	GPIO26	GPIO26	FSPICS4	1	R, USB
GPIO27	26	GPIO27	GPIO27	FSPICS5	3*	R, USB

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up registor enabled (OE = 1, WPU = 1)
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is

0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
1, input enabled, in high impedance state (IE = 1)

- **3*** - input enabled, pull-up resistor enabled (IE = 1, WPU = 0, USB_WPU = 1). See details in Notes

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design, or enable internal pull-up and pull-down resistors during software initialization.

Notes

- **R** - These pins have analog functions.
- **USB** - USB pull-up resistor enabled
  - By default, the USB function is enabled for USB pins (i.e., GPIO26 and GPIO27), and the pin pull-up is decided by the USB pull-up. The USB pull-up is controlled by USB_SERIAL_JTAG _DP/DM_PULLUP and the pull-up resistor value is controlled by USB_SERIAL_JTAG_PULLUP_VALUE. For details, see *ESP32-H2 Technical Reference Manual* > Chapter *USB Serial/JTAG Controller*.
  - When the USB function is disabled, USB pins are used as regular GPIOs and the pin's internal weak pull-up and pull-down resistors are disabled by default (configurable by IO_MUX_GPIO*n*_FUN_WPU/WPD). For details, see *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix (GPIO, IO MUX)*).

2.9 ADC

It is recommended to add a 0.1 μF filter capacitor between pins and ground when using the ADC function.

2.10 USB

ESP32-H2 integrates a USB serial/JTAG controller that is compatible with USB 2.0 full-speed mode.

GPIO26 and GPIO27 can be used as D- and D+ for USB, and it is recommended to add a series resistor (initial value can be 0 Ω) and a capacitor to ground (initially optional), and place them near the ESP32-H2 chip.

ESP32-H2 also supports downloading and log printing through USB. For instructions on download over USB, please refer to Section 4.3.

3 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-H2 PCB layout using the ESP32-H2-MINI-1 module as an example.

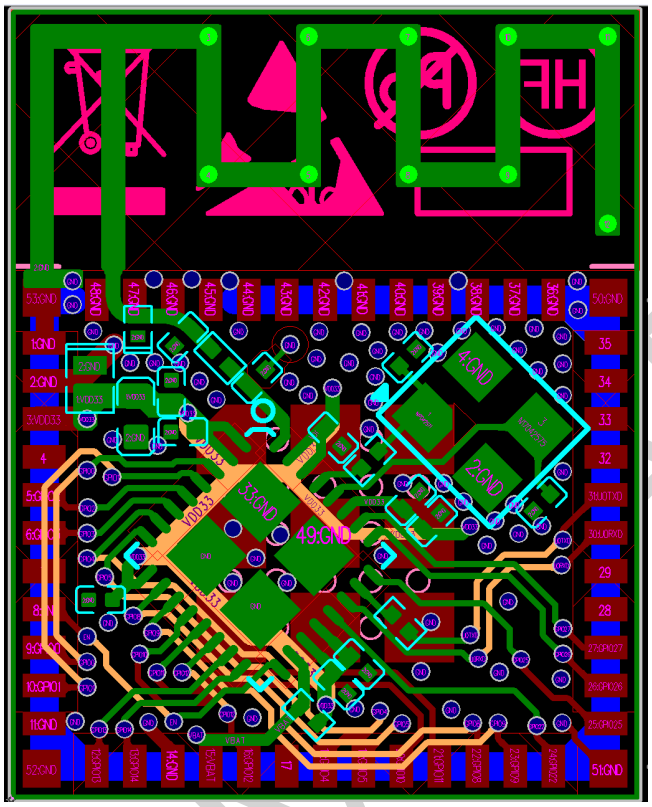

Figure 10: ESP32-H2 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓are strongly recommended, while positions without a mark are not recommended.

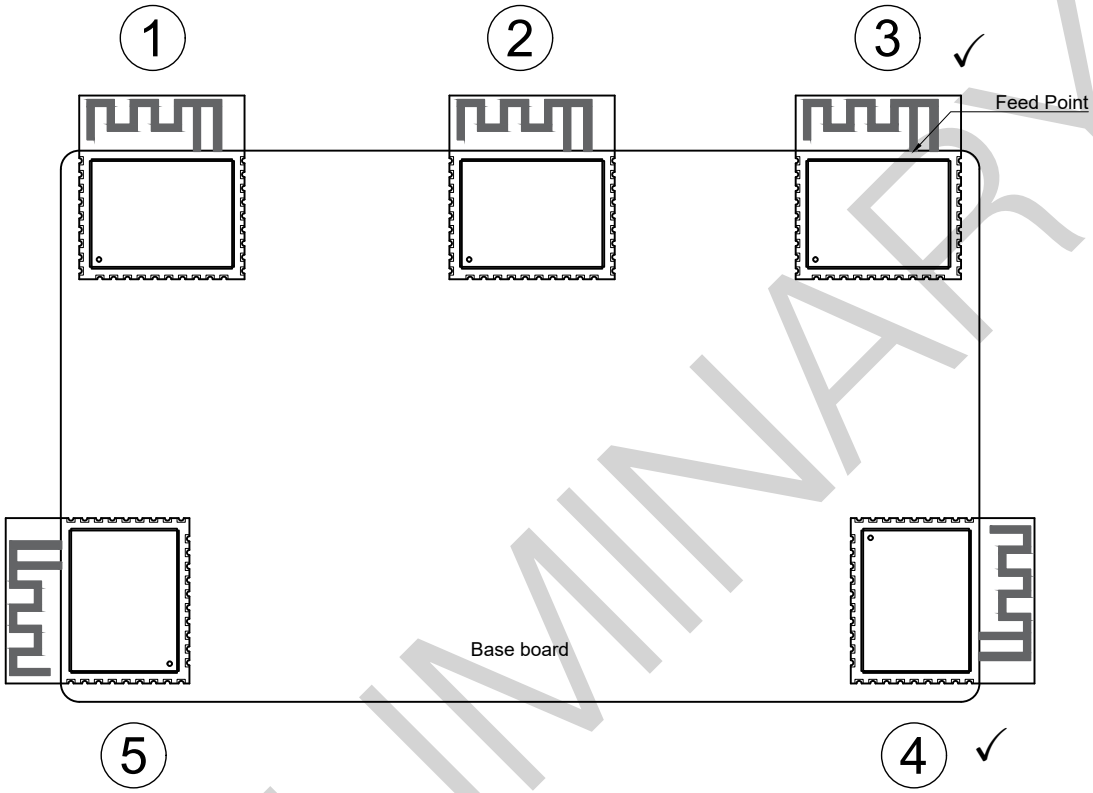

Figure 11: Placement of ESP32-H2 Modules on Base Board (antenna feed point on the right)

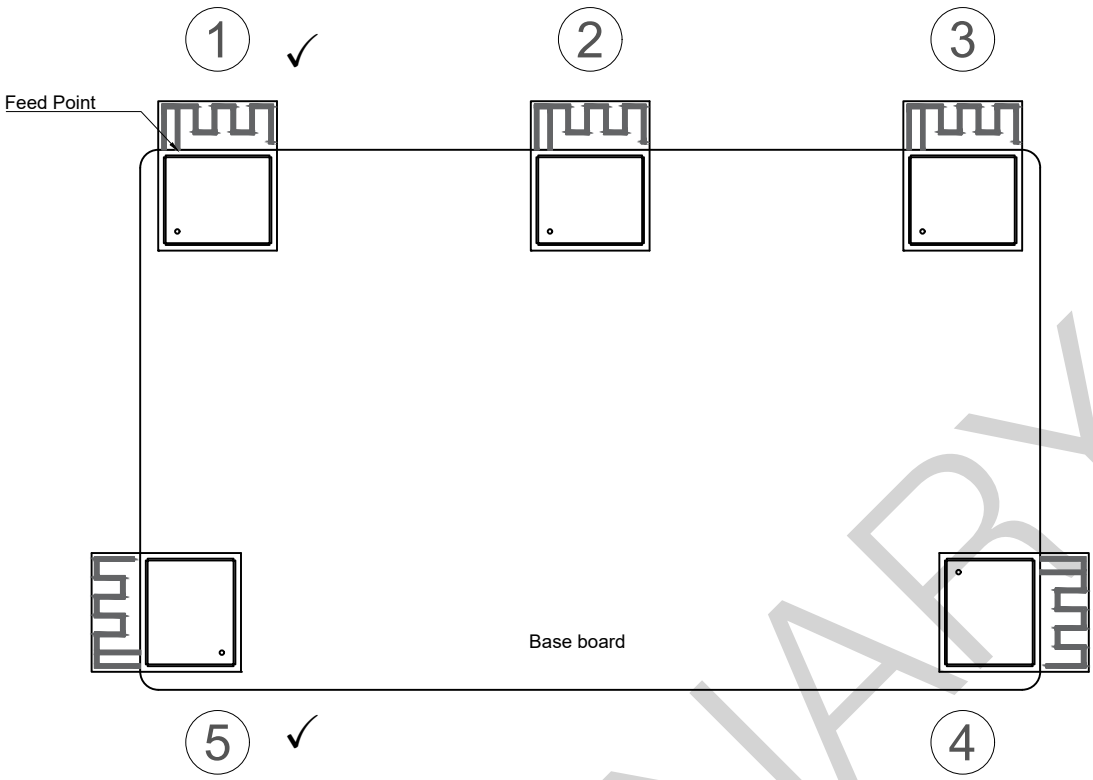

Figure 12: Placement of ESP32-H2 Modules on Base Board (antenna feed point on the left)

If PCB antenna could not be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure 13 shows the suggested clearance for modules whose antenna feed point is on the left.

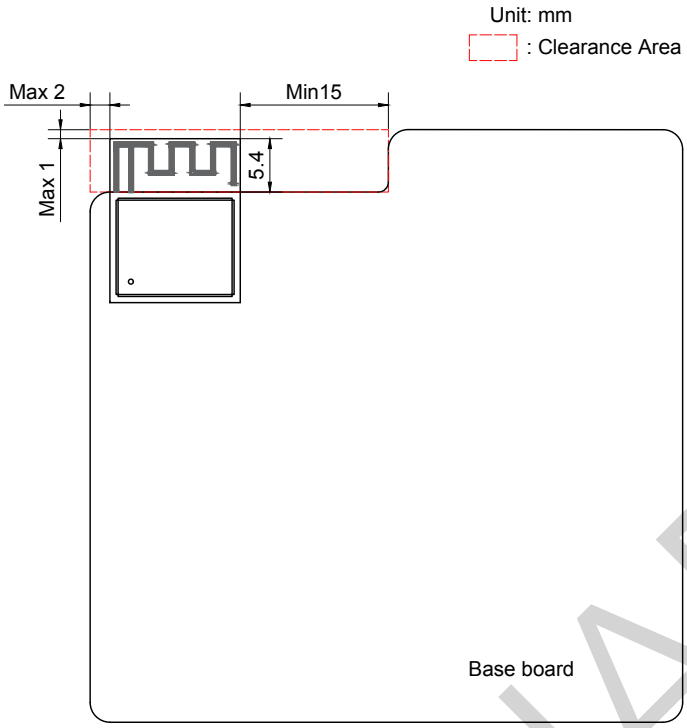

Figure 13: Keepout Zone for ESP32-H2 Module's Antenna on the Base Board

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

3.3 Power Supply

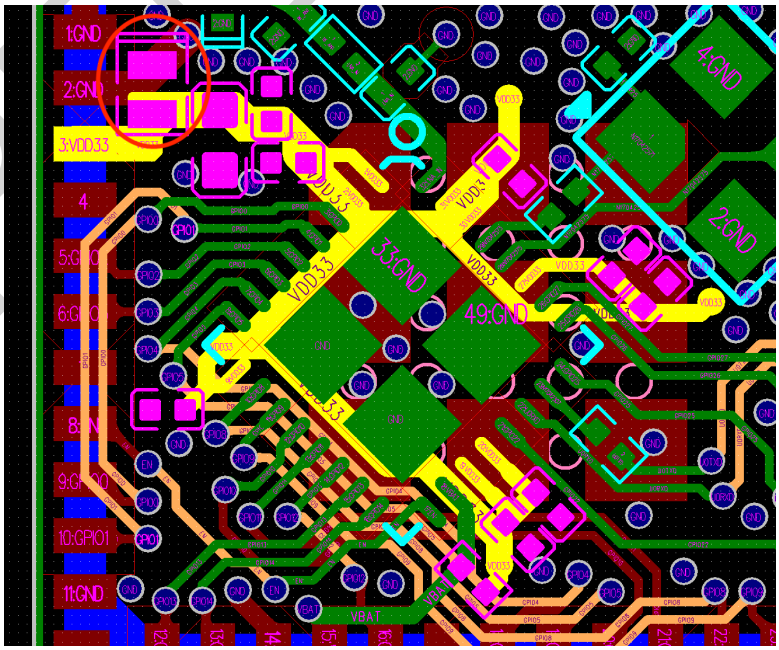

Figure 14: ESP32-H2 Power Traces in a Four-layer PCB Design

- Four-layer PCB design is preferred. The power traces should be routed on the inner third layer whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 14. The width of the main power traces should be no less than 20 mil. The width of the power traces for VDD3P3 pins should be no less than 15 mil. Recommended width of other power traces is 10 mil.
- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 14). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction. After that, the power traces are divided into several branches using a star-shape topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor's ground pad to ensure a short return path.

  Notice:
  In Figure 14, the 10 μF capacitor is shared by the analog power supply pin1 VDD3P3, pin2 VDD3P3, and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near the VDD3P3 pin, it is recommended to add a 10 μF capacitor to both the chip power entrance and the analog power VDD3P3, and also reserve a 1 μF capacitor if space permits.

- Pin1 VDD3P3 and pin2 VDD3P3 analog power supply should be surrounded by ground copper. It is required to add GND isolation between the pin1 VDD3P3, pin2 VDD3P3, power trace and the surrounding GPIO and RF traces, and place vias whenever possible.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 14. This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate.

3.4 Crystal

Figure 15 and Figure 16 show the reference design of the crystal. The crystal can be either connected to the ground or not in the top layer. If there is sufficient ground in the top layer, it is recommended not to connect the crystal to the ground. This helps to reduce the value of parasitic capacitance and suppress temperature conduction, which can otherwise affect the frequency offset. In addition, the following should be noted:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 1.8 mm**. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- Components in series to the crystal trace should be placed close to the chip side.

- The external matching capacitors should be placed on the two sides of the crystal, not connected directly to the series components, and at the end of the clock trace, to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

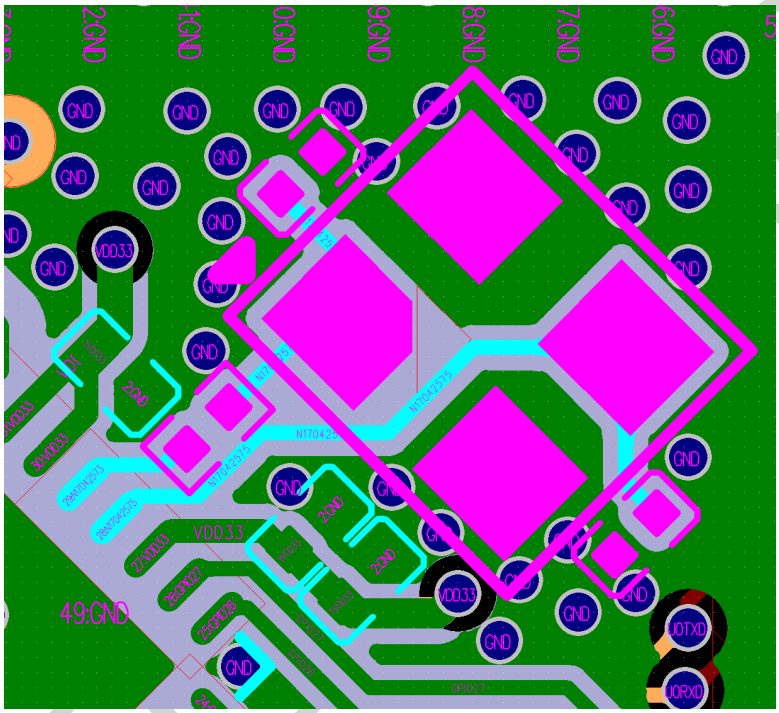

Figure 15: ESP32-H2 Crystal Oscillator Layout (Connected to the Ground)

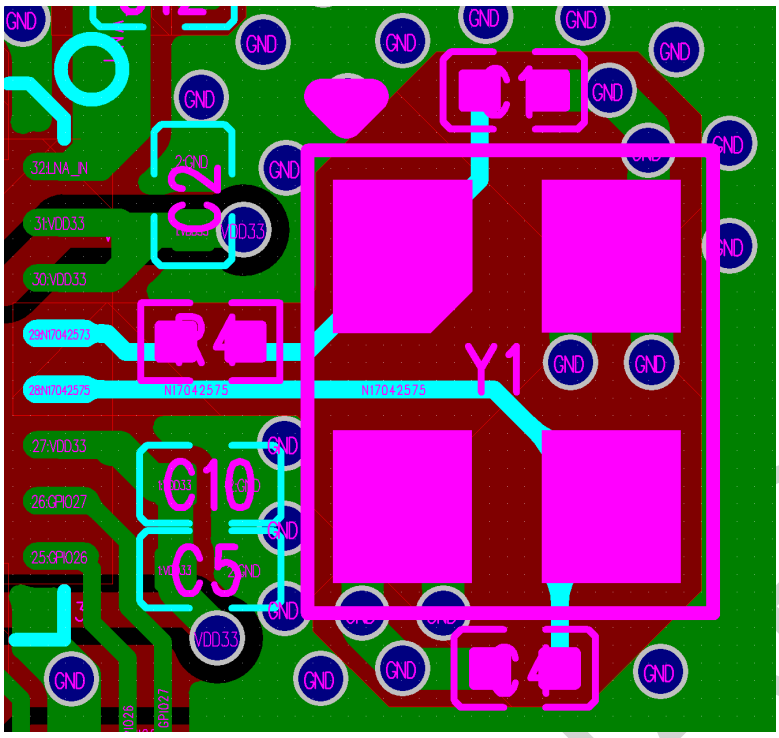

Figure 16: ESP32-H2 Crystal Oscillator Layout (Not Connected to the Ground)

3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 17.

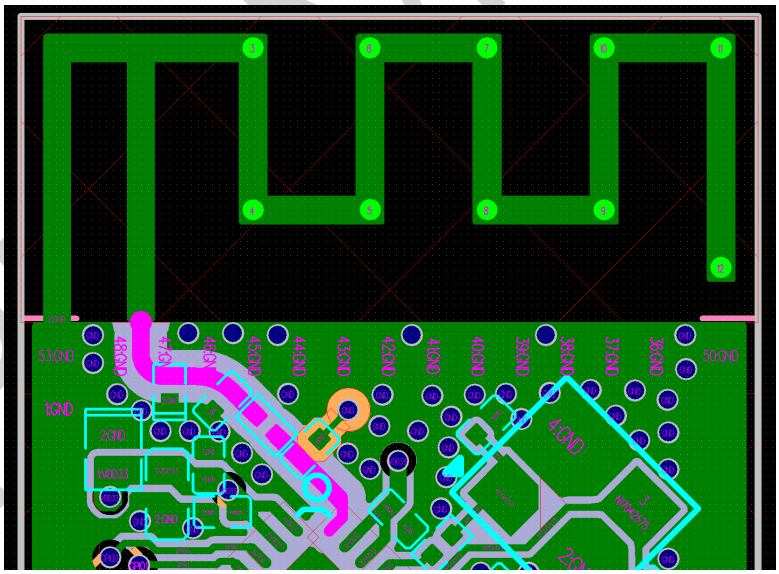

Figure 17: ESP32-H2 RF Layout in a Four-layer PCB Design

- The RF trace should have 50 Ω characteristic impedance. The reference plane is the second layer. A π-type matching circuit should be added on the RF trace and placed close to the chip, in a zigzag.
- For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown in Figure 18.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Figure 18: ESP32-H2 PCB Stack up Design

- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for inteference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub to ground at the ground pad of the first matching capacitor to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 19 is the stub. Note that a stub is not required for package types above 0201.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

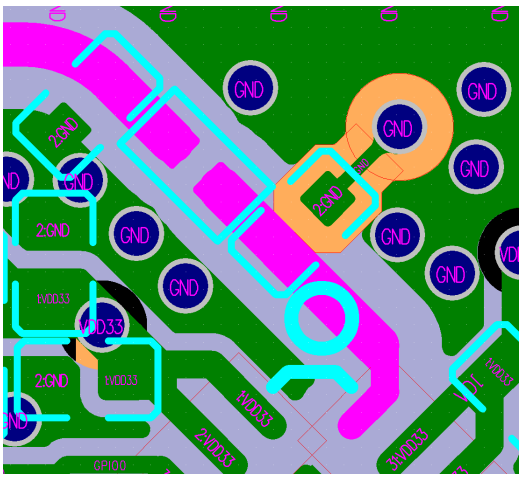

Figure 19: ESP32-H2 Stub in a Four-layer PCB Design

3.6 UART

- The series resistor on the U0TXD trace needs to be placed close to the ESP32-H2 chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

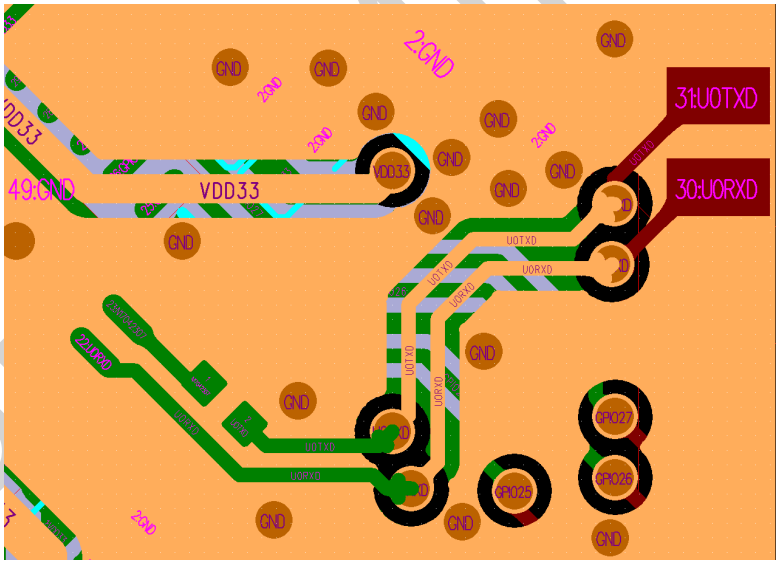

Figure 20: ESP32-H2 UART0 Layout

3.7 USB

- Place the RC circuit on the USB traces close to the ESP32-H2 chip side.
- Please use differential pairs and route them in parallel at equal lengths.
- Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

3.8 Typical Layout Problems and Solutions

3.8.1 Q: The voltage ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The voltage ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-H2 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-H2 sends MCS7@11n packets, and <120 mV when ESP32-H2 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable voltage ripples.

3.8.2 Q: The voltage ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.8.3 Q: When ESP32-H2 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.8.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.

4 Hardware Development

4.1 ESP32-H2 Modules

For a list of ESP32-H2 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

4.2 ESP32-H2 Development Boards

For a list of the latest designs of ESP32-H2 boards please check Development Boards section of Espressif website.

4.3 Download Guidelines

You can download firmware to ESP32-H2 either via UART or USB.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, i.e., strapping pin GPIO8 (floating by default) is pulled high and pin GPIO9 (pulled up by default) is pulled low.
2. Power up the chip or module and check the log via UART0 serial port. If the log shows “waiting for download”, the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using Flash Download Tool.
4. After firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. Perform the download from step 3 if there is working program firmware in the flash. Otherwise, make sure to set the chip or module to Joint Download Boot mode, i.e., strapping pin GPIO8 (floating by default) is pulled high and pin GPIO9 (pulled up by default) is pulled low.
2. Power up the chip or module and check the log via USB serial port. If the log shows “waiting for download”, the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via USB using Flash Download Tool.
4. After firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the module again. The chip will read and execute the new firmware during initialization.

Notice:

- It is advised to download the firmware only after the “waiting for download” log shows via serial ports.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one com port.
- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip to Joint Download Boot mode first by configuring the strapping pin.

  - USB PHY is disabled by the application;
  - USB is secondary developed for other USB functions, e.g., USB host, USB standard device;
  - USB GPIOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.

5 Related Documentation and Resources

Related Documentation

- ESP32-H2 Series Datasheet – Specifications of the ESP32-H2 hardware.
- ESP32-H2 Technical Reference Manual – Detailed information on how to use the ESP32-H2 memory and peripherals.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-H2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-H2
- *ESP32-H2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-H2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-H2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-H2 Series SoCs* – Browse through all ESP32-H2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-H2
- *ESP32-H2 Series Modules* – Browse through all ESP32-H2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-H2
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  https://espressif.com/en/products/devkits?id=ESP32-H2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Glossary

CLC	Capacitor-Inductor-Capacitor
DDR	Double-Data Rate
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
SiP	System-in-Package
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Revision History

Date	Version	Release Notes
2023-08-02	v0.7	• Improved the description in a note of Section 2.2.3; • Updated the description about Boot Mode Control in Section 2.7; • Renamed Download Boot mode to Joint Download Boot mode; • Updated a typo in the note about USB under Table 5.
2023-06-29	v0.6	• Updated Section 2.5 to add recommended values for the chip RF matching circuit; • Updated the note about "chip RF matching circuit" in Section 2.5, and Figure 1, Figure 2, Figure 3, and Figure 7; • Updated the note about USB under Table 5; • Renamed RTC clock to low-power clock.
2023-05-24	v0.5	Preliminary release

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