ESP8684 Series

Datasheet

Ultra-Low-Power SoC with RISC-V Single-Core CPU

Supporting IEEE 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth 5 (LE)

1 MB, 2 MB or 4 MB flash in the 4×4 mm QFN package

Including:

ESP8684H1

ESP8684H2

ESP8684H4

Version v1.4

Espressif Systems

Product Overview

ESP8684 series of SoCs is an ultra-low-power and highly-integrated MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). The block diagram of ESP8684 series is shown below.

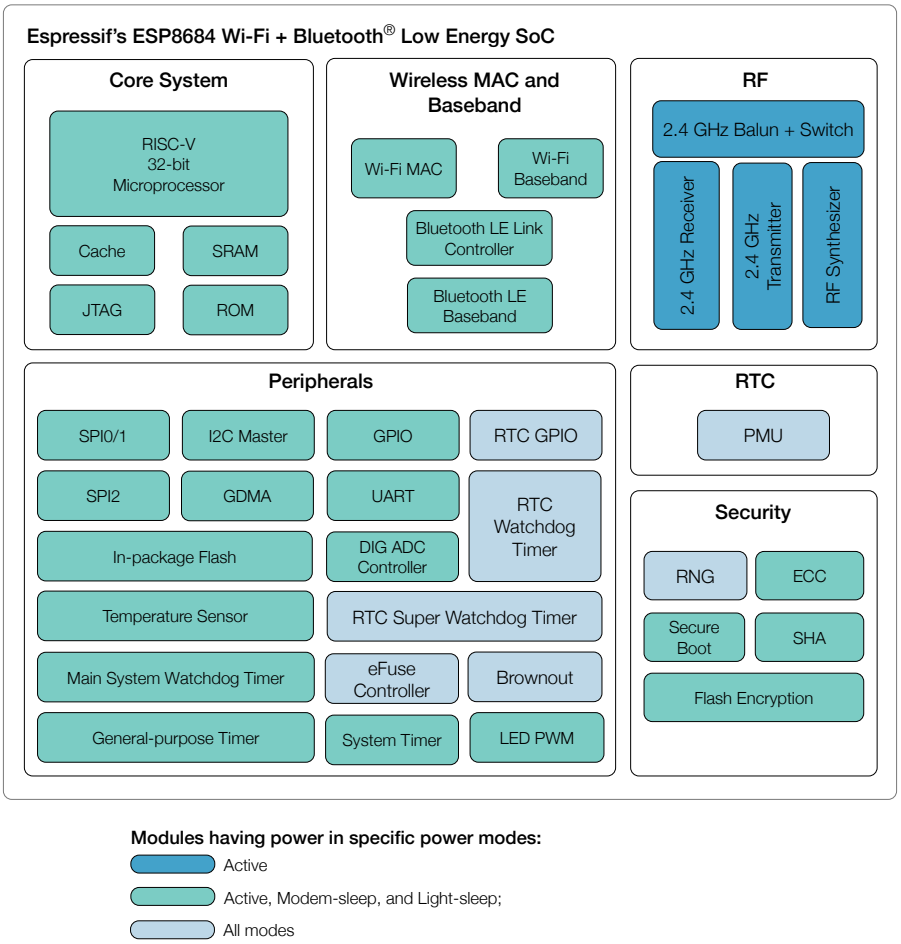

Figure 1: Functional block diagram of ESP8684

Solution Highlights

- **A complete Wi-Fi subsystem** that complies with IEEE 802.11b/g/n protocol and supports Station mode, SoftAP mode, SoftAP + Station mode, and promiscuous mode
- **A Bluetooth LE subsystem** that supports features of Bluetooth 5, central role and peripheral role
- **State-of-the-art power and RF performance**
- **32-bit RISC-V single-core processor** with a four-stage pipeline that operates at up to 120 MHz
- **Storage capacity** ensured by 272 KB of SRAM (16 KB for cache) and 576 KB of ROM on the chip.
- **Reliable security features** ensured by
  - Cryptographic hardware accelerators that support ECC, Hash and secure boot
  - Random number generator
  - External memory encryption and decryption
- **Rich set of peripheral interfaces and GPIOs**, ideal for various scenarios and complex applications

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 72.2 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- 3 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
  Note that when ESP8684 series scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity

Bluetooth

- Bluetooth LE: Bluetooth 5
- High power mode 20 dBm
- Speed: 125 kbps, 500 kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

CPU and Memory

- 32-bit RISC-V single-core processor, up to 120 MHz
- CoreMark® score:
  - 1 core at 120 MHz: 305.42 CoreMark; 2.55 CoreMark/MHz
- 576 KB ROM
- 272 KB SRAM (16 KB for cache)
- In-package flash (see details in Chapter 1 *ESP8684 Series Comparison*)
- Access to flash accelerated by cache
- Supports flash in-Circuit Programming (ICP)

Advanced Peripheral Interfaces

- 14 × programmable GPIOs
- Digital interfaces:
  - 3 × SPI
  - 2 × UART
  - 1 × I2C Master
  - LED PWM controller, with up to 6 channels
  - General DMA controller (GDMA), with 1 transmit channel and 1 receive channel
- Analog interfaces:
  - 1 × 12-bit SAR ADC, up to 5 channels
  - 1 × temperature sensor
- Timers:
  - 1 × 54-bit general-purpose timer
  - 2 × watchdog timers
  - 1 × 52-bit system timer

Low Power Management

- Power Management Unit with four power modes

Security

- Secure boot
- Flash encryption
- 1024-bit OTP, up to 256 bits for use

- Cryptographic hardware acceleration:
  - ECC
  - SHA Accelerator (FIPS PUB 180-4)
- Random Number Generator (RNG)
- Clock glitch filter

Applications (A Non-exhaustive List)

With ultra-low power consumption, ESP8684 is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
  - Indoor positioning
- Industrial Automation
  - Industrial robot
  - Industrial field bus
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Logger toys and proximity sensing toys
- Health Care
  - Health monitor
  - Baby monitor
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agriculture robot
- Retail and Catering
  - POS machines
  - Service robot
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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1 ESP8684 Series Comparison

1.1 ESP8684 Series Nomenclature

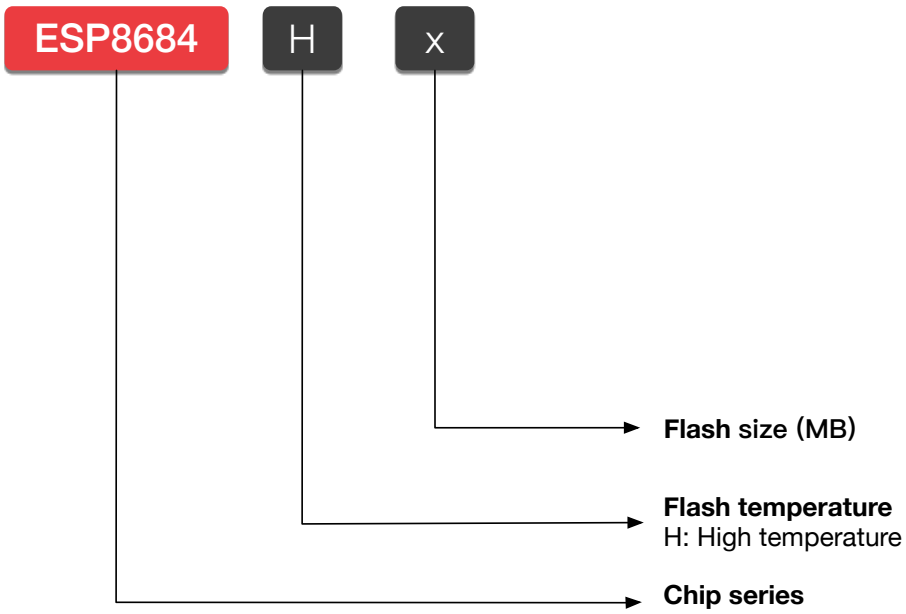

Figure 2: ESP8684 Series Nomenclature

1.2 Comparison

Table 1: ESP8684 Series Member Comparison

Ordering Code	In-Package flash	Ambient Temperature (°C)	Package (mm)
ESP8684H1[1]	1 MB	–40 ~ 105	QFN24 (4*4)
ESP8684H2	2 MB	–40 ~ 105	QFN24 (4*4)
ESP8684H4	4 MB	–40 ~ 105	QFN24 (4*4)

[1] The ESP8684H1 chip is still in **sample status**.

2 Pin Definition

2.1 Pin Layout

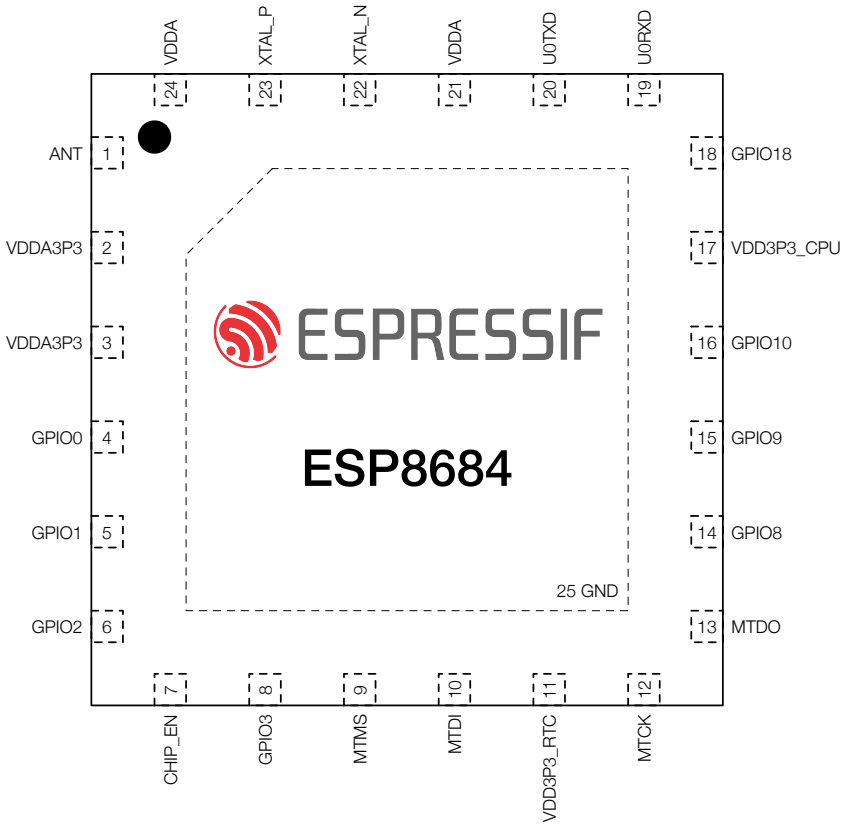

Figure 3: ESP8684 Pin Layout (Top View)

2.2 Pin Description

Table 2: Pin Description

Name	No.	Type	Power Domain	Function
ANT	1	I/O	—	RF input and output
VDDA3P3	2	P_A	—	Analog power supply
VDDA3P3	3	P_A	—	Analog power supply
GPIO0	4	I/O/T	VDD3P3_RTC	**GPIO0**, ADC1_CH0
GPIO1	5	I/O/T	VDD3P3_RTC	**GPIO1**, ADC1_CH1
GPIO2	6	I/O/T	VDD3P3_RTC	**GPIO2**, ADC1_CH2, FSPIQ
CHIP_EN	7	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_EN pin floating.
GPIO3	8	I/O/T	VDD3P3_RTC	**GPIO3**, ADC1_CH3
MTMS	9	I/O/T	VDD3P3_RTC	**MTMS**, GPIO4, ADC1_CH4, FSPIHD
MTDI	10	I/O/T	VDD3P3_RTC	**MTDI**, GPIO5, FSPIWP

Name	No.	Type	Power Domain	Function
VDD3P3_RTC	11	P_D	—	Input power supply for RTC
MTCK	12	I/O/T	VDD3P3_CPU	**MTCK**, GPIO6, FSPICLK
MTDO	13	I/O/T	VDD3P3_CPU	**MTDO**, GPIO7, FSPID
GPIO8	14	I/O/T	VDD3P3_CPU	**GPIO8**
GPIO9	15	I/O/T	VDD3P3_CPU	**GPIO9**
GPIO10	16	I/O/T	VDD3P3_CPU	**GPIO10**, FSPICS0
VDD3P3_CPU	17	P_D	—	Input power supply for digital IO
GPIO18	18	I/O/T	VDD3P3_CPU	**GPIO18**
U0RXD	19	I/O/T	VDD3P3_CPU	**U0RXD**, GPIO19
U0TXD	20	I/O/T	VDD3P3_CPU	**U0TXD**, GPIO20
VDDA	21	P_A	—	Analog power supply
XTAL_N	22	—	—	External crystal output
XTAL_P	23	—	—	External crystal input
VDDA	24	P_A	—	Analog power supply
GND	25	G	—	Ground

[1] P_A: analog power supply; P_D: power supply for digital IO; I: input; O: output; T: high impedance.

[2] Pin functions in bold font are the default pin functions.

[3] The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to Chapter IO MUX and GPIO Matrix (GPIO, IO_MUX) in *ESP8684 Technical Reference Manual*.

2.3 Power Scheme

Digital pins of ESP8684 are divided into two different power domains:

- VDD3P3_CPU
- VDD3P3_RTC

VDD3P3_CPU is the input power supply for digital IO and digital system.

VDD3P3_RTC is the input power supply for RTC, RTC IO, and digital system.

The power scheme diagram is shown in Figure 4.

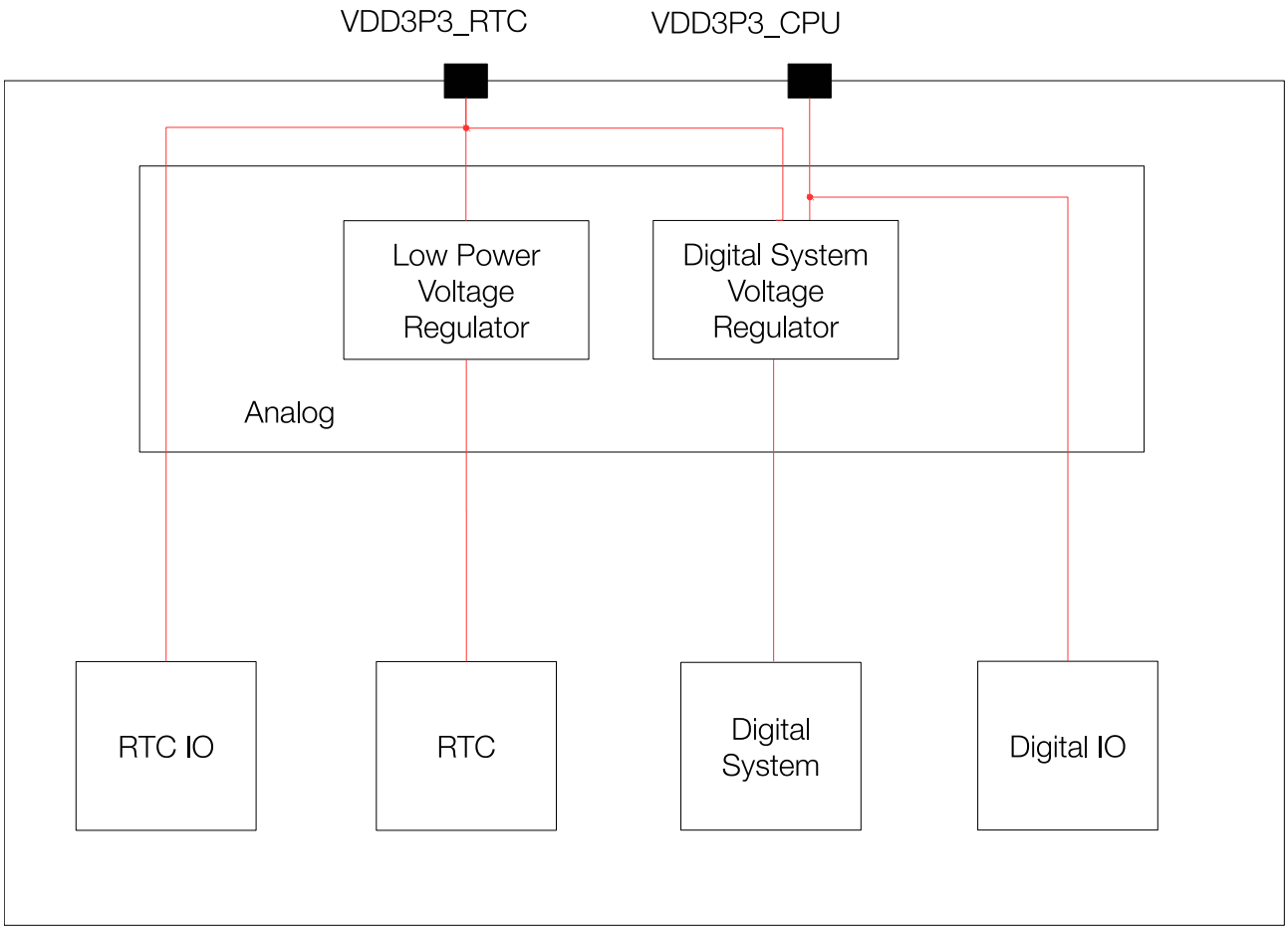

Figure 4: ESP8684 Series Power Scheme

Notes on CHIP_EN:

Figure 5 shows the power-up and reset timing of ESP8684 series. Details about the parameters are listed in Table 3.

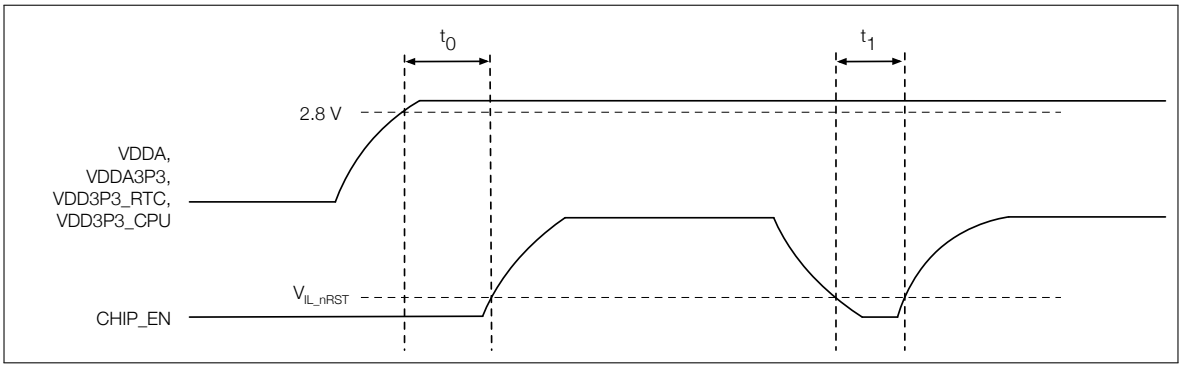

Figure 5: ESP8684 Series Power-up and Reset Timing

Table 3: Description of ESP8684 Series Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDDA3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} (refer to its value in Table 11) to reset the chip	50

2.4 Strapping Pins

ESP8684 series has two strapping pins:

- GPIO8
- GPIO9

Software can read the values of GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register. For register description, please refer to Section GPIO Matrix Register Summary in *ESP8684 Technical Reference Manual*.

During the chip's power-on reset, RTC watchdog reset, and brownout reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

By default, GPIO9 is connected to the internal weak pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1".

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8684.

After reset, the strapping pins work as normal-function pins.

Table 4 lists detailed booting configurations of the strapping pins.

Table 4: Strapping Pins

Booting Mode [1]			
Pin	Default	SPI Boot	Joint Download Boot[2]
GPIO8	N/A	Don't care	1
GPIO9	Internal weak pull-up	1	0
Enabling/Disabling ROM Messages Print During Booting			
Pin	Default	Functionality	
GPIO8	N/A	When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.	

[1] The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

[2] Joint Download Boot mode supports UART Download Boot download method. In addition to SPI Boot and Joint Download Boot modes, ESP8684 also supports SPI Download Boot mode. For details, please see *ESP8684 Technical Reference Manual* > Chapter *Chip Boot Control*.

Figure 6 shows the setup and hold times for the strapping pins before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 5.

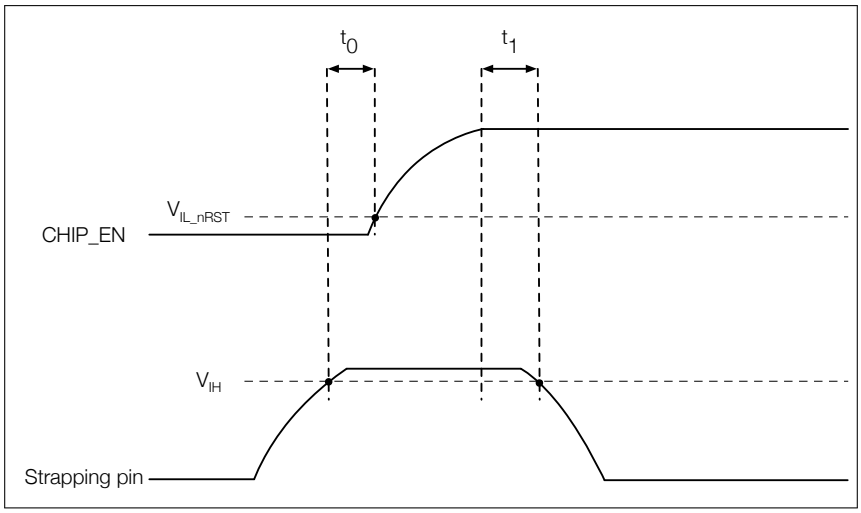

Figure 6: Setup and Hold Times for the Strapping Pins

Table 5: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

3 Functional Description

This chapter describes the functions of ESP8684.

3.1 Radio and Wi-Fi

The ESP8684 series radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

3.1.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP8684 series integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

3.1.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

3.1.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.1.4 Wi-Fi Radio and Baseband

The ESP8684 series Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz bandwidth
- 802.11n 0.4 μs guard interval
- data rate up to 72.2 Mbps
- RX STBC (single spatial stream)
- adjustable transmitting power
- antenna diversity
  ESP8684 series supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.1.5 Wi-Fi MAC

ESP8684 series implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP8684 series Wi-Fi MAC applies the following low-level protocol functions automatically:

- 3 × virtual Wi-Fi interfaces
- infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- transmit opportunity (TXOP)
- Wi-Fi multimedia (WMM)
- CCMP, TKIP, WEP, BIP, WPA2-PSK/WPA2-Enterprise, and WPA3-PSK/WPA3-Enterprise
- automatic beacon monitoring (hardware TSF)

3.1.6 Networking Features

Espressif provides libraries for TCP/IP networking and other networking protocols over Wi-Fi. TLS 1.2 (default) and 1.3 are also supported.

3.2 Bluetooth LE

ESP8684 series includes a Bluetooth Low Energy subsystem that integrates a hardware link layer controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5.

3.2.1 Bluetooth LE Radio and PHY

Bluetooth Low Energy radio and PHY in ESP8684 series support:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- coded PHY for longer range (125 Kbps and 500 Kbps)
- HW listen before talk (LBT)

3.2.2 Bluetooth LE Link Layer Controller

Bluetooth Low Energy Link Layer Controller in ESP8684 series supports:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- multiple advertisement sets
- simultaneous advertising and scanning
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- connection parameter update
- high duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- link layer extended scanner filter policies
- low duty cycle directed advertising
- link layer encryption
- LE Ping

3.3 CPU and Memory

3.3.1 CPU

ESP8684 series has a low-power 32-bit RISC-V single-core microprocessor with the following features:

- four-stage pipeline that supports a clock frequency of up to 120 MHz
- RV32IMC ISA
- 32-bit multiplier and 32-bit divider
- up to 32 vectored interrupts at seven priority levels
- up to 2 hardware breakpoints/watchpoints
- JTAG for debugging

3.3.2 Internal Memory

ESP8684's internal memory includes:

- **576 KB of ROM**: for booting and core functions.
- **272 KB of on-chip SRAM**: for data and instructions, running at a configurable frequency of up to 120 MHz. Of the 272 KB SRAM, 16 KB is configured for cache.
- **1 Kbit of eFuse**: 256 bits are reserved for your data, such as encryption key and device ID.
- **In-package flash** : See details in Chapter 1 *ESP8684 Series Comparison*.

3.3.3 Address Mapping Structure

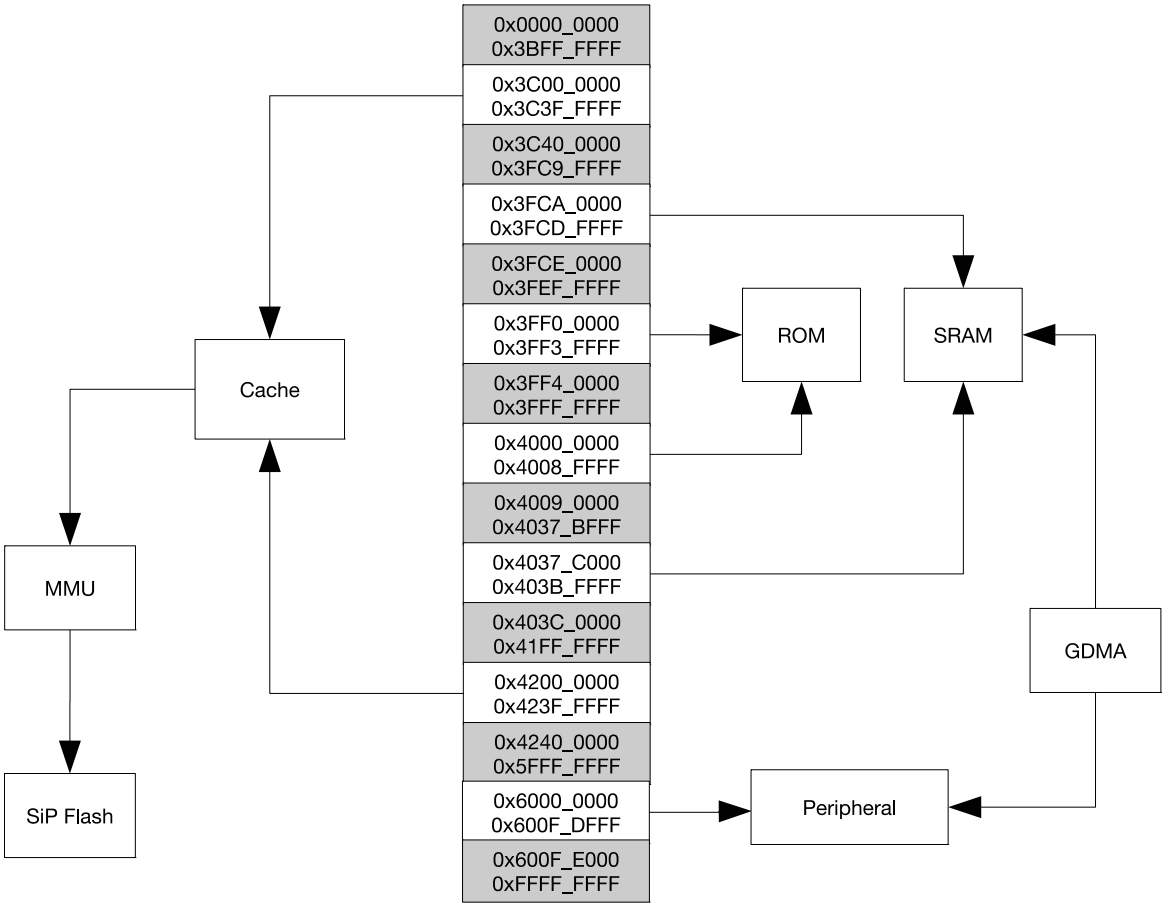

Figure 7: Address Mapping Structure

Note:
The memory space with gray background is not available for use.

3.3.4 Cache

ESP8684 series has an four-way set associative cache. This cache is read-only and has the following features:

- size: 16 KB

- block size: 32 bytes
- critical word first and early restart

3.4 System Clocks

3.4.1 CPU Clock

The CPU clock has three possible sources:

- external main crystal clock
- fast RC oscillator (typically about 17.5 MHz, and adjustable)
- PLL clock

The application can select the clock source from the three clocks above. The selected clock source drives the CPU clock directly, or after division, depending on the application. Once the CPU is reset, the default clock source would be the external main crystal clock divided by 2.

Note:
ESP8684 is unable to operate without an external main crystal clock.

3.4.2 RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller. It has three possible sources:

- internal slow RC oscillator (typically about 136 kHz, and adjustable)
- internal fast RC oscillator divided clock (derived from the fast RC oscillator divided by 256)
- external slow clock (clock signal input through GPIO0, and typically about 32.768 kHz)

The RTC fast clock is used for RTC peripherals and sensor controllers. It has two possible sources:

- external main crystal clock divided by 2
- internal fast RC oscillator clock (typically about 17.5 MHz, and adjustable)

3.5 Digital Peripherals

3.5.1 General Purpose Input / Output Interface (GPIO)

ESP8684 has 14 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pins. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pins while peripheral output signals can be configured to any IO pins. Table 6 shows the IO MUX functions of each pin. For more information about IO MUX and GPIO matrix, please refer to Chapter IO MUX and GPIO Matrix (GPIO, IO_MUX) in *ESP8684 Technical Reference Manual*.

Table 6: IO MUX Pin Functions

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
GPIO0	4	GPIO0	GPIO0	—	0	R, G
GPIO1	5	GPIO1	GPIO1	—	0	R, G
GPIO2	6	GPIO2	GPIO2	FSPIQ	1	R
GPIO3	8	GPIO3	GPIO3	—	1	R, G
MTMS	9	MTMS	GPIO4	FSPIHD	1	R
MTDI	10	MTDI	GPIO5	FSPIWP	1	R, G
MTCK	12	MTCK	GPIO6	FSPICLK	1*	—
MTDO	13	MTDO	GPIO7	FSPID	1	—
GPIO8	14	GPIO8	GPIO8	—	1	—
GPIO9	15	GPIO9	GPIO9	—	3	—
GPIO10	16	GPIO10	GPIO10	FSPICS0	1	—
GPIO18	18	GPIO18	GPIO18	—	0	—
U0RXD	19	U0RXD	GPIO19	—	3	—
U0TXD	20	U0TXD	GPIO20	—	4	—

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
  0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
  1, input enabled, in high impedance state (IE = 1)

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design referring to Table 11, or enable internal pull-up and pull-down resistors during software initialization.

Notes

- **R** - These pins have analog functions.
- **G** - These pins have glitches during power-up. See details in Table 7.

Table 7: Power-Up Glitches on Pins

Pin	Glitch[1]	Typical Time Period (μs)
GPIO0	Low-level glitch	40
GPIO1	Low-level glitch	60
GPIO3	Low-level glitch	40
MTDI	Low-level glitch	60

[1] Low-level glitch: the pin is at a low level during the time period;

3.5.2 Serial Peripheral Interface (SPI)

ESP8684 series features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can be configured to operate in SPI memory mode and SPI2 can be configured to operate in general-purpose SPI mode.

- **SPI Memory mode**

  In SPI memory mode, SPI0 and SPI1 interface with in-package flash. Data is transferred in bytes. Up to four-line STR reads and writes are supported. The clock frequency is configurable to a maximum of 60 MHz in STR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. SPI2 supports two-line full-duplex communication and single-/two-/four-line half-duplex communication in both master and slave modes. The host's clock frequency of SPI2 is configurable. Data is transferred in bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface can connect to GDMA.

  In master or slave mode, the clock frequency is 40 MHz at most, and the four modes of SPI transfer format are supported.

3.5.3 Universal Asynchronous Receiver Transmitter (UART)

ESP8684 series has two UART interfaces, i.e. UART0 and UART1, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 2.5 Mbps. The UART controller provides hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF).

3.5.4 I2C Interface

ESP8684 series has an I2C bus master interface. The I2C interface supports:

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- double addressing mode
- 7-bit broadcast address

You can configure instruction registers to control the I2C interface for more flexibility.

3.5.5 LED PWM Controller

The LED PWM controller has the following features:

- Six identical, independent PWM generators (i.e. channels) that generate digital waveforms
- Configurable waveform periods and duty cycle
- Maximum PWM resolution: 14 bits
- PWM signal output in low-power mode (Light-sleep mode)
- Automatic duty cycle fading - gradual increase/decrease of PWM duty cycle, which is useful for the LED RGB color-gradient generator.

3.5.6 General DMA Controller

ESP8684 series has a general DMA controller (GDMA) with two independent channels, i.e. one transmit channel and one receive channel. These two channels are shared by peripherals with DMA feature. The GDMA controller implements a fixed-priority scheme among these channels, whose priority can be configured.

The GDMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal RAM.

Peripherals on ESP8684 series with DMA feature are SPI2 and SHA.

3.6 Analog Peripherals

3.6.1 Analog-to-Digital Converter (ADC)

ESP8684 series integrates a 12-bit SAR ADC, which supports measurements on 5 channels.

For ADC characteristics, please refer to Table 12.

3.6.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –40 °C to 125 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the operating ambient temperature.

3.7 Timers

3.7.1 General Purpose Timer

ESP8684 series is embedded with a 54-bit general-purpose timer, which is based on a 16-bit prescaler and a 54-bit auto-reload-capable up/down-timer.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 2 to 65536
- a 54-bit time-base counter programmable to be incrementing or decrementing

- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- level interrupt generation

3.7.2 System Timer

ESP8684 series integrates a 52-bit system timer, which has two 52-bit counters and three comparators. The system timer has the following features:

- counters with a fixed clock frequency of 16 MHz
- three types of independent interrupts generated according to alarm value
- two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- automatic reload of counter value
- counters can be stalled if the CPU is stalled or in OCD mode

3.7.3 Watchdog Timers

The ESP8684 series contains two watchdog timers: one in general-purpose timer group (called Main System Watchdog Timer, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and MWDT are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

3.8 Low Power Management

With the use of advanced power-management technologies, ESP8684 series can switch between different power modes.

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. Wireless base band, and radio are disabled, but wireless connection can remain active.

- Light-sleep mode: The CPU is paused. Any wake-up events (MAC,RTC timer, or external interrupts) will wake up the chip. Wireless connection can remain active.
- Deep-sleep mode: CPU and most peripherals are powered down. Only the PMU in RTC power management unit is powered on. For more details, please refer to Figure 1.

For power consumption in different power modes, please refer to Current Consumption.

3.9 Cryptographic Hardware Accelerators

ESP8684 series is equipped with hardware accelerators of general algorithms, such as:

- SHA1/SHA224/SHA256 (FIPS PUB 180-4)
- ECC

3.10 Physical Security Features

- In-package flash encryption (AES-XTS algorithm) with software inaccessible key prevents unauthorized readout of your application code or data.
- Secure boot feature uses a hardware root of trust to ensure only signed firmware can be booted.
- The clock glitch filter can filter the glitches on the external main crystal clock, so as to prevent the chip from being attacked by clock glitches.

3.11 Peripheral Pin Configurations

Table 8: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO0	One 12-bit SAR ADC
	ADC1_CH1	GPIO1	
	ADC1_CH2	GPIO2	
	ADC1_CH3	GPIO3	
	ADC1_CH4	MTMS	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	Any GPIO pins	Two UART channels with hardware flow control
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		

Interface	Signal	Pin	Function
	U1RTS_out		
	U1DTR_out		
I2C	I2CEXT0_SCL_in	Any GPIO pins	One I2C channel in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
LED PWM	ledc_ls_sig_out0~5	Any GPIO pins	Six independent PWM channels
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	• Master mode and slave mode of SPI, Dual SPI, Quad SPI, and QPI • Connection to external flash, RAM, and other SPI devices • Four modes of SPI transfer format • Configurable SPI frequency • 64-byte FIFO or GDMA buffer
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA3P3, VDDA, VDD3P3_RTC, VDD3P3_CPU	Voltage applied to power supply pins per power domain	–0.3	3.6	V
I_{output} [1]	Cumulative IO output current	—	730	mA
T_{STORE}	Storage temperature	–40	150	°C

[1] The chip worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in two domains (VDD3P3_RTC, VDD3P3_CPU) output high logic level to ground.

4.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA3P3, VDDA, VDD3P3_RTC, VDD3P3_CPU[1]	Voltage applied to power supply pin	3.0	3.3	3.6	V
I_{VDD}[2]	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	-40	—	105	°C

[1] To write eFuse, VDD3P3_CPU should not be higher than 3.3 V.

[2] If you use a single power supply, the recommended output current is 500 mA or more.

4.3 DC Characteristics (3.3 V, 25 °C)

Table 11: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA

I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for a particular power domain of pins.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.4 ADC Characteristics

Table 12: ADC Characteristics

Symbol	Parameter	Min	Max	Unit
DNL (Differential nonlinearity)[1]	ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi off	–1	3	LSB
INL (Integral nonlinearity)		–4	8	LSB
Sampling rate	—	—	100	kSPS [2]

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

ESP-IDF provides a couple of calibration methods for ADC. Results after calibration using hardware + software calibration are shown in Table 13. For higher accuracy, users may apply other calibration methods provided in ESP-IDF, or implement their own.

Table 13: ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 950	-5	5	mV
	ATTEN3, effective measurement range of 0 ~ 2800	-10	10	mV

4.5 Current Consumption

4.5.1 RF Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 14: Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @22 dBm	370
		802.11g, 54 Mbps, @20 dBm	320
		802.11n, HT20, MCS7, @19 dBm	300
	RX	802.11b/g/n, HT20	65

Table 15: Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 20.0 dBm	320
		Bluetooth LE @ 9.0 dBm	190
		Bluetooth LE @ 0 dBm	150
		Bluetooth LE @ –15.0 dBm	90
	RX	Bluetooth LE	62

4.5.2 Current Consumption in Other Modes

Table 16: Current Consumption in Low-Power Modes

Work mode	Description	Typ	Unit
Light-sleep	—	140	μA
Deep-sleep	Only RTC timer is powered on	5	μA
Power off	CHIP_EN is set to low level, and the chip is powered off	1	μA

Table 17: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	80	WFI (Wait-for-Interrupt)	9.4	10.3
		CPU run at full speed	12.1	13.0
	120	WFI (Wait-for-Interrupt)	10.7	11.5
		CPU run at full speed	14.7	15.6

[1] Current consumption when all peripheral clocks are **disabled**.

[2] Current consumption when all peripheral clocks are **enabled**. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

4.6 Reliability

Table 18: Reliability Qualifications

Test Item	Test Conditions	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1] ± 2000 V	JS-001
	CDM (Charge Device Mode)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113
TCT (Temperature Cycling Test)	–65 °C / 150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103
LTSL (Low Temperature Storage Life)	–40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4.7 Wi-Fi Radio

Table 19: Wi-Fi Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2412	—	2484

4.7.1 Wi-Fi RF Transmitter (TX) Specifications

Table 20: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	21.5	—
802.11b, 11 Mbps	—	21.5	—
802.11g, 6 Mbps	—	21.5	—
802.11g, 54 Mbps	—	19.5	—

Cont'd on next page

Table 20 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT20, MCS0	—	21.0	—
802.11n, HT20, MCS7	—	19.0	—

Table 21: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @21.5 dBm	—	–25.2	–10
802.11b, 11 Mbps, @21.5 dBm	—	–25.2	–10
802.11g, 6 Mbps, @21.5 dBm	—	–20.4	–5
802.11g, 54 Mbps, @19.5 dBm	—	–26.8	–25
802.11n, HT20, MCS0, @21 dBm	—	–21.0	–5
802.11n, HT20, MCS7, @19 dBm	—	–29.0	–27

[1] SL stands for standard limit value.

4.7.2 Wi-Fi RF Receiver (RX) Specifications

Table 22: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–99.0	—
802.11b, 2 Mbps	—	–96.5	—
802.11b, 5.5 Mbps	—	–94.0	—
802.11b, 11 Mbps	—	–90.0	—
802.11g, 6 Mbps	—	–94.0	—
802.11g, 9 Mbps	—	–92.0	—
802.11g, 12 Mbps	—	–91.0	—
802.11g, 18 Mbps	—	–89.0	—
802.11g, 24 Mbps	—	–86.0	—
802.11g, 36 Mbps	—	–83.0	—
802.11g, 48 Mbps	—	–78.5	—
802.11g, 54 Mbps	—	–77.0	—
802.11n, HT20, MCS0	—	–92.5	—
802.11n, HT20, MCS1	—	–90.5	—
802.11n, HT20, MCS2	—	–87.5	—
802.11n, HT20, MCS3	—	–84.5	—
802.11n, HT20, MCS4	—	–81.5	—
802.11n, HT20, MCS5	—	–77.5	—
802.11n, HT20, MCS6	—	–75.5	—
802.11n, HT20, MCS7	—	–74.0	—

Table 23: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	-1	—

Table 24: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	16	—

4.8 Bluetooth LE Radio

Table 25: Bluetooth LE Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2402	—	2480

4.8.1 Bluetooth LE RF Transmitter (TX) Specifications

Table 26: Transmitter General Characteristics

Parameter	Description	Min	Typ	Max	Unit
RF transmit power[1]	RF power control range	–24.0	—	20.0	dBm

[1] Target center frequency range and transmit power are configurable by software. See ESP RF Test Tool and Test Guide for more details.

Table 27: Transmitter Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	1.0	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	2.3	—	kHz

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Table 27 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Max $\|f_n - f_{n-5}\|$	—	1.4	—	kHz
	$\|f_1 - f_0\|$	—	1.5	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.2	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	234.4	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	1.0	—	—
In-band spurious emissions	± 2 MHz offset	—	–32	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–41	—	dBm

Table 28: Transmitter Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\,1,\,2,\,..k}$	—	3.7	—	kHz
	Max $\|f_0 - f_n\|$	—	1.8	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.5	—	kHz
	$\|f_1 - f_0\|$	—	1.1	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	500.0	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	460.7	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	1.0	—	—
In-band spurious emissions	± 4 MHz offset	—	–40	—	dBm
	± 5 MHz offset	—	–43	—	dBm
	> ± 5 MHz offset	—	–44	—	dBm

Table 29: Transmitter Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\,1,\,2,\,..k}$	—	0.6	—	kHz
	Max $\|f_0 - f_n\|$	—	0.7	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.4	—	kHz
	$\|f_0 - f_3\|$	—	0.7	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.0	—	kHz
	Min $\Delta f1_{max}$ (for at least 99.9% of all$\Delta f2_{max}$)	—	241.0	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–32	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–41	—	dBm

Table 30: Transmitter Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\,1,\,2,\,..k}$	—	0.5	—	kHz
	Max $\|f_0 - f_n\|$	—	0.6	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.2	—	kHz
	$\|f_0 - f_3\|$	—	0.8	—	kHz
Modulation characteristics	$\Delta\, f2_{avg}$	—	251.3	—	kHz
	Min $\Delta\, f2_{max}$ (for at least 99.9% of all $\Delta\, f2_{max}$)	—	234.5	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–32	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–41	—	dBm

4.8.2 Bluetooth LE RF Receiver (RX) Specifications

Table 31: Receiver Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–98.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-1	—	dB
	F = F0 – 1 MHz	—	-3	—	dB
	F = F0 + 2 MHz	—	–26	—	dB
	F = F0 – 2 MHz	—	–28	—	dB
	F = F0 + 3 MHz	—	–34	—	dB
	F = F0 – 3 MHz	—	–33	—	dB
	F >= F0 + 4 MHz	—	–33	—	dB
	F <= F0 – 4 MHz	—	–31	—	dB
Image frequency	—	—	–33	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–32	—	dB
	F = F_{image} – 1 MHz	—	–34	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–23	—	dBm
	2003 MHz ~ 2399 MHz	—	–30	—	dBm
	2484 MHz ~ 2997 MHz	—	–10	—	dBm
	3000 MHz ~ 12.75 GHz	—	–17	—	dBm
Intermodulation	—	—	–31	—	dBm

Table 32: Receiver Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–95.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB

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Table 32 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	–11	—	dB
	F = F0 – 2 MHz	—	–7	—	dB
	F = F0 + 4 MHz	—	–35	—	dB
	F = F0 – 4 MHz	—	–30	—	dB
	F = F0 + 6 MHz	—	–35	—	dB
	F = F0 – 6 MHz	—	–29	—	dB
	F >= F0 + 8 MHz	—	–39	—	dB
	F <= F0 – 8 MHz	—	–33	—	dB
Image frequency	—	—	–35	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–35	—	dB
	F = F_{image} – 2 MHz	—	–11	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–30	—	dBm
	2003 MHz ~ 2399 MHz	—	–34	—	dBm
	2484 MHz ~ 2997 MHz	—	–19	—	dBm
	3000 MHz ~ 12.75 GHz	—	–28	—	dBm
Intermodulation	—	—	–33	—	dBm

Table 33: Receiver Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–106.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-7	—	dB
	F = F0 – 1 MHz	—	-5	—	dB
	F = F0 + 2 MHz	—	–35	—	dB
	F = F0 – 2 MHz	—	–34	—	dB
	F = F0 + 3 MHz	—	–38	—	dB
	F = F0 – 3 MHz	—	–37	—	dB
	F >= F0 + 4 MHz	—	–41	—	dB
	F <= F0 – 4 MHz	—	–45	—	dB
Image frequency	—	—	–41	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–43	—	dB
	F = F_{image} – 1 MHz	—	–38	—	dB

Table 34: Receiver Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–102.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-6	—	dB

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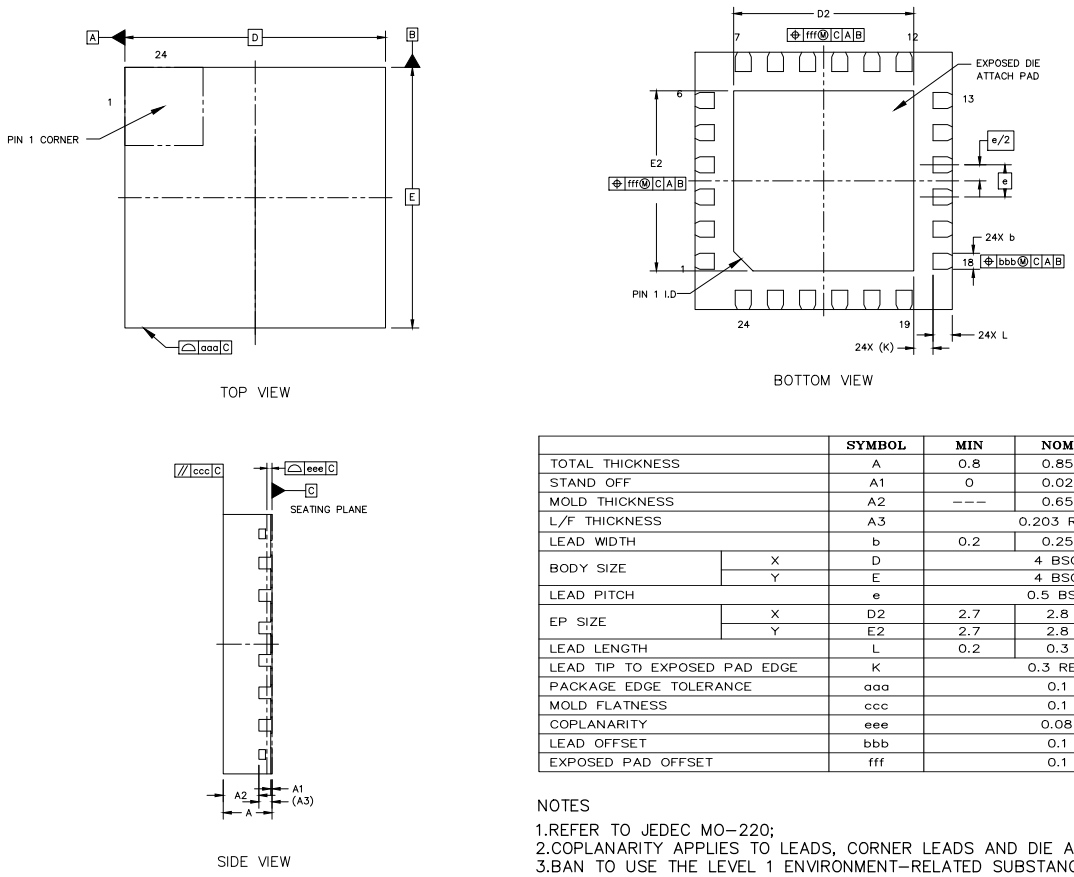
Table 34 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	F = F0 – 1 MHz	—	-5	—	dB
	F = F0 + 2 MHz	—	–29	—	dB
	F = F0 – 2 MHz	—	–32	—	dB
	F = F0 + 3 MHz	—	–31	—	dB
	F = F0 – 3 MHz	—	–36	—	dB
	F >= F0 + 4 MHz	—	–34	—	dB
	F <= F0 – 4 MHz	—	–33	—	dB
Image frequency	—	—	–34	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–37	—	dB
	F = F_{image} – 1 MHz	—	–31	—	dB

5 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP · Sn8~20s

Figure 8: QFN24 (4×4 mm) Package

Note:

- All dimensions are in millimeters (mm).
- The pins of the chip are numbered in a clockwise direction from Pin 1 in the top view;
- Please go to Chipsets to view the recommended PCB package source file (asc). The source file can be imported using software such as PADS or AD (Altium Designer);
- For information about tape, reel, and product marking, please refer to *Espressif Chip-Packing Information*.

6 Related Documentation and Resources

Related Documentation

- ESP8684 Technical Reference Manual – Detailed information on how to use the ESP8684 memory and peripherals.
- ESP8684 Hardware Design Guidelines – Guidelines on how to integrate the ESP8684 into your hardware product.
- ESP8684 Series SoC Errata – Descriptions of errors in ESP8684 series of SoCs from chip revision 0 forward.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP8684 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP8684
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP8684 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
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Revision History

Date	Version	Release notes
2023-10-31	v1.4	Added current consumption for Bluetooth LE in Active mode in Table 15
2023-07-25	v1.3	• Updated table 1 • Renamed ”SiP Flash” to ”In-package Flash” to keep term consistency • Added information about clock glitch filter in Section *Physical Security Features* • Added SRAM clock frequency in Section *Internal Memory*.
2022-12-13	v1.2	Updated table 24
2022-12-08	v1.1	Delete feature ”Supports external power amplifier”
2022-10-24	v1.0	• Updated section *ADC Characteristics*. • Added section *Reliability*. • Updated section *Bluetooth LE Radio* • Added link to the recommended PCB package source file.
2022-07-12	v0.7	Added table ”power-up glitches on pins” for *General Purpose Input / Output Interface (GPIO)*
2022-06-30	v0.6	Updated *Current Consumption in Other Modes*
2022-05-05	v0.5	Updated *Wi-Fi Radio* and *Bluetooth LE Radio*
2022-01-28	v0.4	Updated *Electrical Characteristics* and *Package Information*
2021-12-22	v0.2	Updated section Applications
2021-11-30	v0.1	Preliminary release

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